

MODEL NAME : LA-F371P non-AR  
PCB NO : DAA000EC010  
BOM P/N : 431A8C31L01

# Dell/Compal Confidential

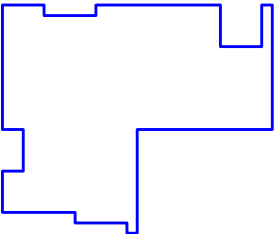
## Schematic Document

Pebble Creek MLK (Kabylake R/U)

2017-11-03

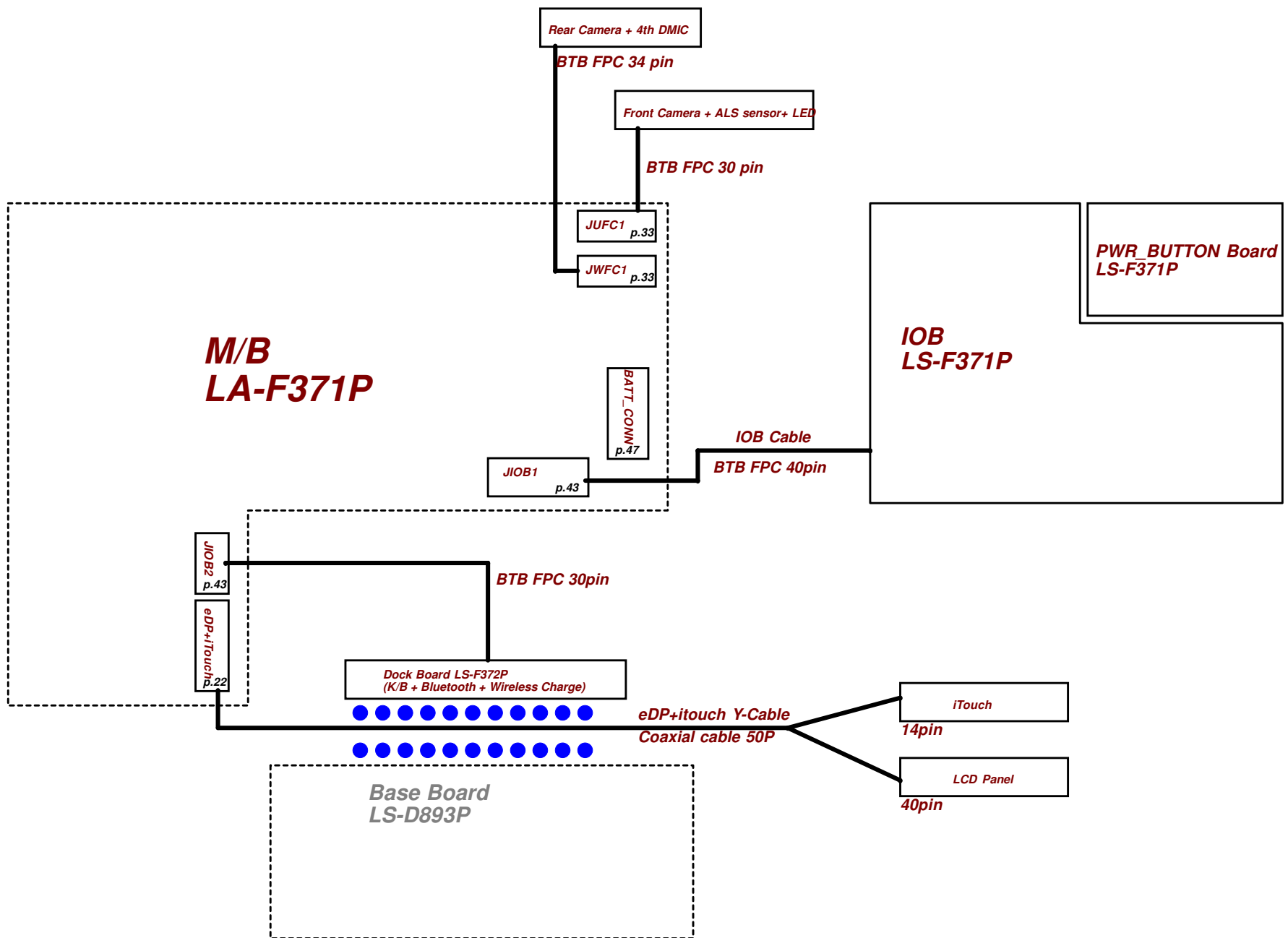
Rev: 1.0

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MB\_PCB



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				Size	Document Number	Rev
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Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	240K +/- 5%	4700p		
1	130K +/- 5%	4700p	Pre-EVT1	
2	62K +/- 5%	4700p	EVT1	
3	33K +/- 5%	4700p	DVT1	
4	8.2K +/- 5%	4700p	DVT2	
5	4.3K +/- 5%	4700p	PVT	
6	2K +/- 5%	4700p		
7	NC			

Board ID Table

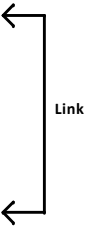
Board ID	PCB Revision
0	
1	0.1
2	0.2
3	0.3
4	0.4
5	1.0
6	
7	

USB 3.0

Flexible I/O	Interface	DESTINATION
1	USB 3.0 #1	USB Type-C Port-A
2	USB 3.0 #2/SSIC	NGFF (WWAN)
3	USB 3.0 #3	USB 3.0 Type-A
4	USB 3.0 #4	USB Type-C Port-B
5	PCI-E#1 / USB 3.0#5	Reserved for AR
6	PCI-E#2 / USB 3.0#6	Reserved for AR
7	PCI-E #3	Reserved for AR
8	PCI-E #4	Reserved for AR
9	PCI-E #5	NGFF (WLAN)
10	PCI-E #6	
11	PCI-E #7	NGFF (SSD)
12	PCI-E #8 /SATA #1	NGFF (SSD) #7/#8 2lane PCI-E
13	PCI-E #9	Card Reader
14	PCI-E #10	
15	PCI-E #11	NGFF (WWAN/2nd SSD)
16	PCI-E #12	NGFF (WWAN/2nd SSD)

SMBUS Control Table

	SOURCE	Base	BATT	Charger	XDP	USH	PD Controller	Trinity Dock	P-Sensor	MUX	IMVP	IO Expendor
No use	PCH_SML0CLK PCH_SML0DATA	PCH										
	PCH_SML1CLK PCH_SML1DATA	PCH										
	SMBCLK SMBDATA	PCH			V							
	EC_SMB00_CLK EC_SMB00_DAT	MECS105				V	V			V		
	EC_SMB01_CLK EC_SMB01_DAT	MECS105									V	
	EC_SMB02_CLK EC_SMB02_DAT	MECS105		V								V
	EC_SMB03_CLK EC_SMB03_DAT	MECS105										
	EC_SMB04_CLK EC_SMB04_DAT	MECS105					V		V	V		
	EC_SMB05_CLK EC_SMB05_DAT	MECS105	V					V				
	EC_SMB10_CLK EC_SMB10_DAT	MECS105		V								



Port Mapping USB 2.0 CLK

USB 2.0 PORT#	DESTINATION
1	Type-C Port-A
2	Dock
3	Type-C Port-B
4	WWAN
5	IR CAM
7	WLAN
9	USB Type-A
10	USH

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	
	CLKOUT_PCIE1	NGFF (WLAN)
	CLKOUT_PCIE2	NGFF (WWAN)
	CLKOUT_PCIE3	SSD
	CLKOUT_PCIE5	Card Reader
	FLEX CLOCKS	DESTINATION
	CLKOUT_LPC_0	ESPI
	CLKOUT_LPC_1	ESPI

Displayport

	DDI PORT#	DESTINATION
DDI	1	USB Type-C Port-B
	2	USB Type-C Port-A

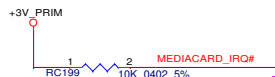
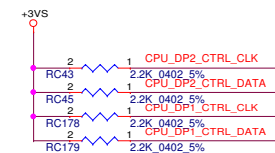
Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

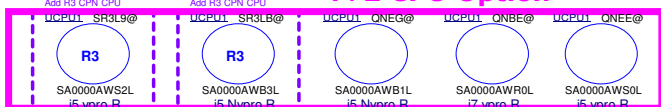
⏏ : means Analog Ground

### Type-C PortA



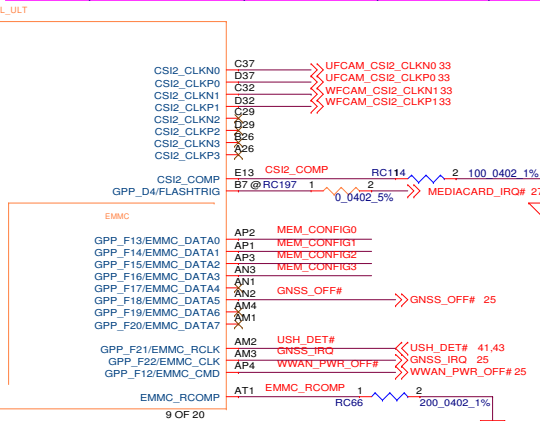
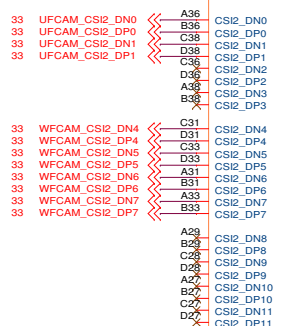
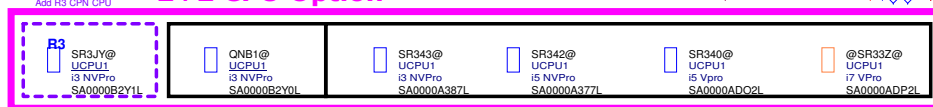
COMPENSATION PU FOR eDP  
CAD Note:Trace width=20 mils, Isolati on Space  
Max length=100 mils.

## 4+2 CPU Option



SKL-U Ballout Rev0.71 &amp; INTEL symbol Rev1.0

















































































## 2+2 CPU Option



## DDR Memory Configuration Type Strapping



GPIO Pin	Pin Name	1866Mbps	Micron 8G	Micron 16G	Micron 32G	Hynix 8G	Hynix 16G	Hynix 32G	Samsung 8G	Samsung 16G	Samsung 32G	2133Mbps	Micron 32G	Hynix 32G	Samsung 32G	Micron 16G	Hynix 16G	Samsung 16G	
GPP_F13	MEM_CONFIG0		0	1	0	1	0	1	0	1	0		1	0	1	0	1	0	
GPP_F14	MEM_CONFIG1		0	0	1	1	0	0	1	1	0		0	1	0	1	1	0	1
GPP_F15	MEM_CONFIG2		0	0	0	0	1	1	1	1	1		0	0	0	0	1	1	1
GPP_F16	MEM_CONFIG3		0	0	0	0	0	0	0	0	0		1	1	1	1	1	1	1

X76		DRAM Option (R1) , R3 check P08				DRAM Config Option			
						MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3
X7669231L05	<div> MICRON_8G@ UD1 MT52L256M32D1PF-107WT SA00009XUOL</div>	<div> MICRON_8G@ UD2 MT52L256M32D1PF-107WT SA00009XUOL</div>	<div> MICRON_8G@ UD3 MT52L256M32D1PF-107WT SA00009XUOL</div>	<div> MICRON_8G@ UD4 MT52L256M32D1PF-107WT SA00009XUOL</div>	<div> X76_M8G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_M8G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_M8G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_M8G@ RH18 10K 0402 5% SD028100280</div>	
X7669231L07	<div> MICRON_16G@ UD1 MT52L512M32D2PF-107WT SA00009U70L</div>	<div> MICRON_16G@ UD2 MT52L512M32D2PF-107WT SA00009U70L</div>	<div> MICRON_16G@ UD3 MT52L512M32D2PF-107WT SA00009U70L</div>	<div> MICRON_16G@ UD4 MT52L512M32D2PF-107WT SA00009U70L</div>	<div> X76_M16G@ RH17 10K 0402 5% SD028100280</div>	<div> X76_M16G@ RH16 10K 0402 5% SD028100280</div>	<div> X76_M16G@ RH13 10K 0402 5% SD028100280</div>	<div> X76_M16G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L09	<div> MICRON_32G@ UD1 MT52L1G32D4PG-107WT SA00009XYOL</div>	<div> MICRON_32G@ UD2 MT52L1G32D4PG-107WT SA00009XYOL</div>	<div> MICRON_32G@ UD3 MT52L1G32D4PG-107WT SA00009XYOL</div>	<div> MICRON_32G@ UD4 MT52L1G32D4PG-107WT SA00009XYOL</div>	<div> X76_M32G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_M32G@ RH15 10K 0402 5% SD028100280</div>	<div> X76_M32G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_M32G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L06	<div> HYNIX_8G@ UD1 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L</div>	<div> HYNIX_8G@ UD2 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L</div>	<div> HYNIX_8G@ UD3 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L</div>	<div> HYNIX_8G@ UD4 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L</div>	<div> X76_H8G@ RH17 10K 0402 5% SD028100280</div>	<div> X76_H8G@ RH15 10K 0402 5% SD028100280</div>	<div> X76_H8G@ RH13 10K 0402 5% SD028100280</div>	<div> X76_H8G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L08	<div> HYNIX_16G@ UD1 H9CCNNNBUTMLAR-NUD FBGA SA00008FJ4L</div>	<div> HYNIX_16G@ UD2 H9CCNNNBUTMLAR-NUD FBGA SA00008FJ4L</div>	<div> HYNIX_16G@ UD3 H9CCNNNBUTMLAR-NUD FBGA SA00008FJ4L</div>	<div> HYNIX_16G@ UD4 H9CCNNNBUTMLAR-NUD FBGA SA00008FJ4L</div>	<div> X76_H16G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_H16G@ RH16 10K 0402 5% SD028100280</div>	<div> X76_H16G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_H16G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L10	<div> HYNIX_32G@ UD1 H9CCNNCLTMLAR-NUD FBGA SA0000AENOL</div>	<div> HYNIX_32G@ UD2 H9CCNNCLTMLAR-NUD FBGA SA0000AENOL</div>	<div> HYNIX_32G@ UD3 H9CCNNCLTMLAR-NUD FBGA SA0000AENOL</div>	<div> HYNIX_32G@ UD4 H9CCNNCLTMLAR-NUD FBGA SA0000AENOL</div>	<div> X76_H32G@ RH17 10K 0402 5% SD028100280</div>	<div> X76_H32G@ RH16 10K 0402 5% SD028100280</div>	<div> X76_H32G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_H32G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L01	<div> X76_BG@ X76BG X76 SAMSUNG_8G@ UD1 K4E6E304EB-EGCF FBGA178K SA00009XYOL</div>	<div> SAMSUNG_8G@ UD2 K4E6E304EB-EGCF FBGA178K SA00009XYOL</div>	<div> SAMSUNG_8G@ UD3 K4E6E304EB-EGCF FBGA178K SA00009XYOL</div>	<div> SAMSUNG_8G@ UD4 K4E6E304EB-EGCF FBGA178K SA00009XYOL</div>	<div> X76_S8G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_S8G@ RH15 10K 0402 5% SD028100280</div>	<div> X76_S8G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_S8G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L02	<div> X76_16G@ X7616G X76 SAMSUNG_16G@ UD1 K4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_16G@ UD2 K4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_16G@ UD3 K4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_16G@ UD4 K4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> X76_S16G@ RH17 10K 0402 5% SD028100280</div>	<div> X76_S16G@ RH16 10K 0402 5% SD028100280</div>	<div> X76_S16G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_S16G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L03	<div> X76_32G@ X7632G X76 SAMSUNG_32G@ UD1 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_32G@ UD2 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_32G@ UD3 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_32G@ UD4 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> X76_S32G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_S32G@ RH16 10K 0402 5% SD028100280</div>	<div> X76_S32G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_S32G@ RH10 10K 0402 5% SD028100280</div>	
X7669231L03	<div> X76_32G@ X7632G X76 SAMSUNG_32G@ UD1 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_32G@ UD2 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_32G@ UD3 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> SAMSUNG_32G@ UD4 4E6E304EB-EGCF FBGA178K SA00008QV2L</div>	<div> X76_S32G@ RH18 10K 0402 5% SD028100280</div>	<div> X76_S32G@ RH16 10K 0402 5% SD028100280</div>	<div> X76_S32G@ RH12 10K 0402 5% SD028100280</div>	<div> X76_S32G@ RH10 10K 0402 5% SD028100280</div>	

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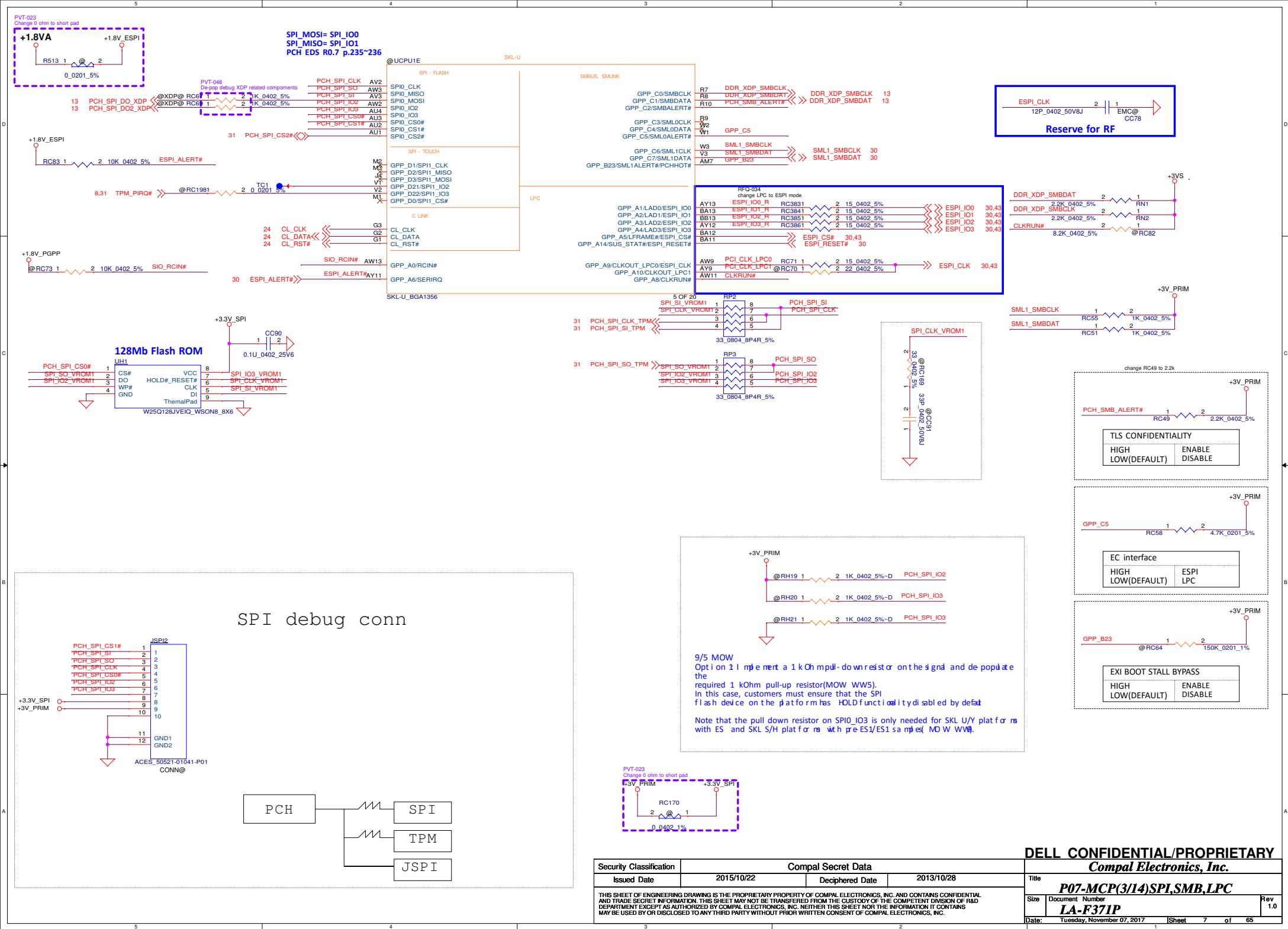
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19	DDR_A_D[0..63]	↔	20	DDR_B_D[0..63]	↔
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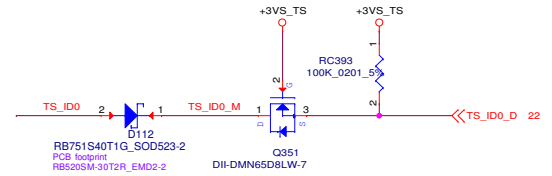
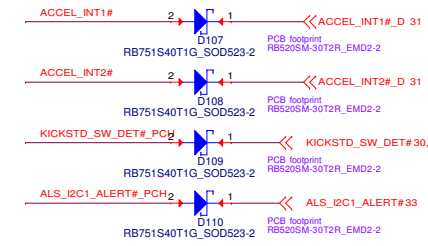
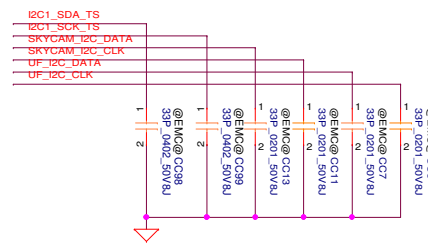
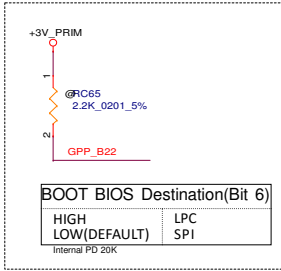
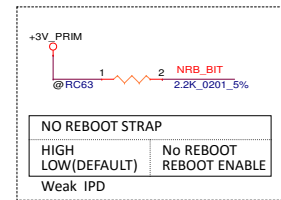
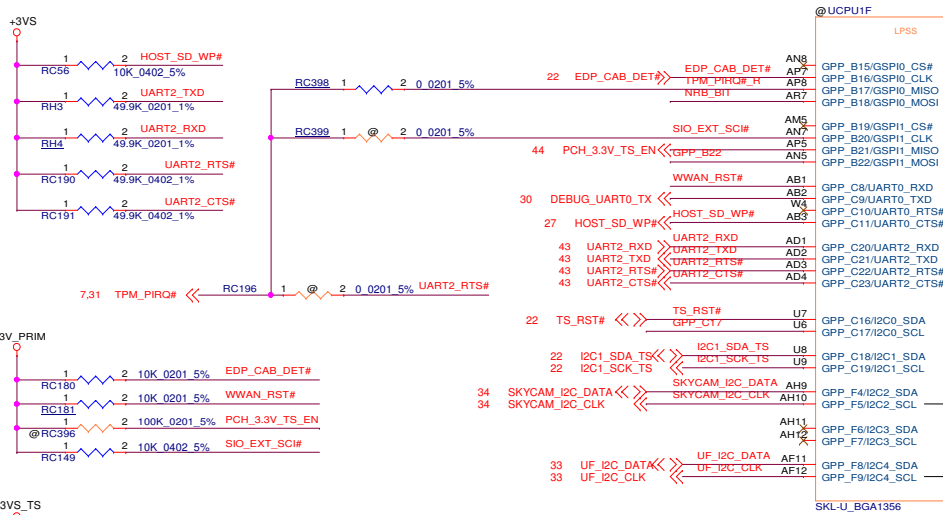
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SM_RCOMP1	RC1661	2	80.6	0402	1%		
SM_RCOMP2	RC1651	2	162	0402	1%		

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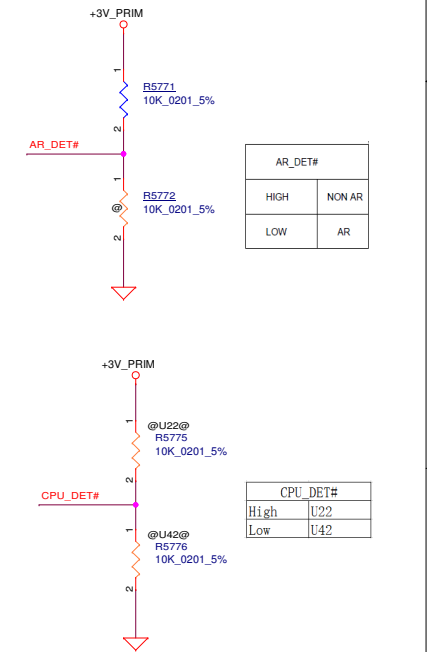
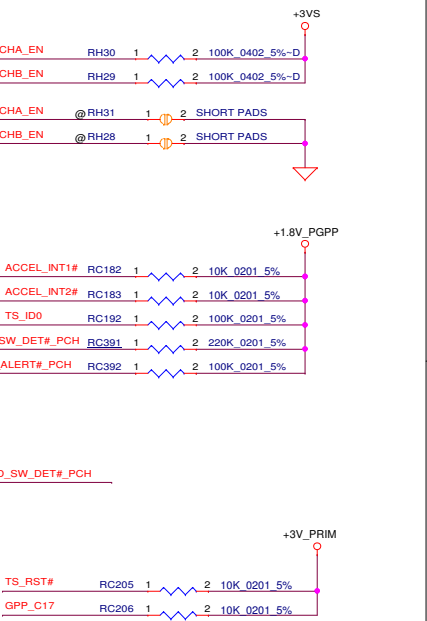
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X76		DRAM Option (R3)			
X7669231L56	Micron 8G/1866	MICRON_8G_R3@ UD1	MICRON_8G_R3@ UD2	MICRON_8G_R3@ UD3	MICRON_8G_R3@ UD4
X7669231L52	Micron 16G/1866	MICRON_16G_R3@ UD1	MICRON_16G_R3@ UD2	MICRON_16G_R3@ UD3	MICRON_16G_R3@ UD4
X7669231L54	Micron 32G/1866	MICRON_32G_R3@ UD1	MICRON_32G_R3@ UD2	MICRON_32G_R3@ UD3	MICRON_32G_R3@ UD4
X7669231L51	Hynix 8G/1866	HYNIX_8G_R3@ UD1	HYNIX_8G_R3@ UD2	HYNIX_8G_R3@ UD3	HYNIX_8G_R3@ UD4
X7669231L53	Hynix 16G/1866	HYNIX_16G_R3@ UD1	HYNIX_16G_R3@ UD2	HYNIX_16G_R3@ UD3	HYNIX_16G_R3@ UD4
X7669231L55	Hynix 32G/1866	HYNIX_32G_R3@ UD1	HYNIX_32G_R3@ UD2	HYNIX_32G_R3@ UD3	HYNIX_32G_R3@ UD4
X7669231L57	Samsung 8G/1866	SAMSUNG_8G_R3@ UD1	SAMSUNG_8G_R3@ UD2	SAMSUNG_8G_R3@ UD3	SAMSUNG_8G_R3@ UD4
X7669231L58	Samsung 16G/1866	SAMSUNG_16G_R3@ UD1	SAMSUNG_16G_R3@ UD2	SAMSUNG_16G_R3@ UD3	SAMSUNG_16G_R3@ UD4
X7669231L59	Samsung 32G/1866	SAMSUNG_32G_R3@ UD1	SAMSUNG_32G_R3@ UD2	SAMSUNG_32G_R3@ UD3	SAMSUNG_32G_R3@ UD4

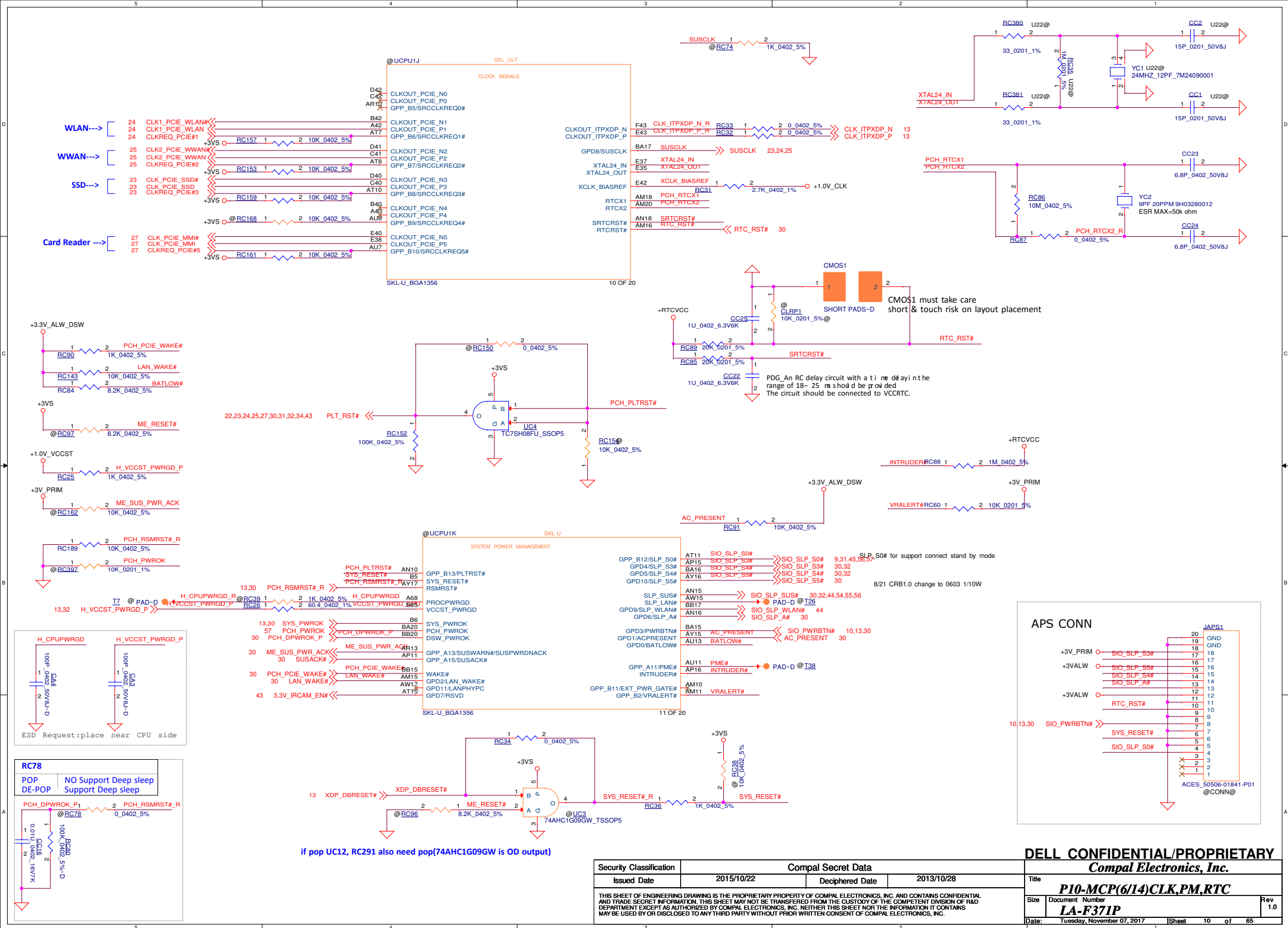


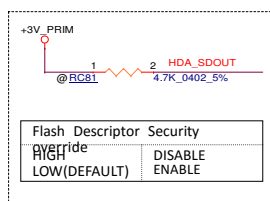
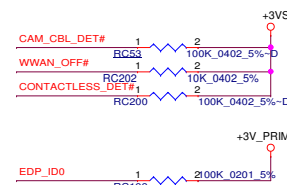
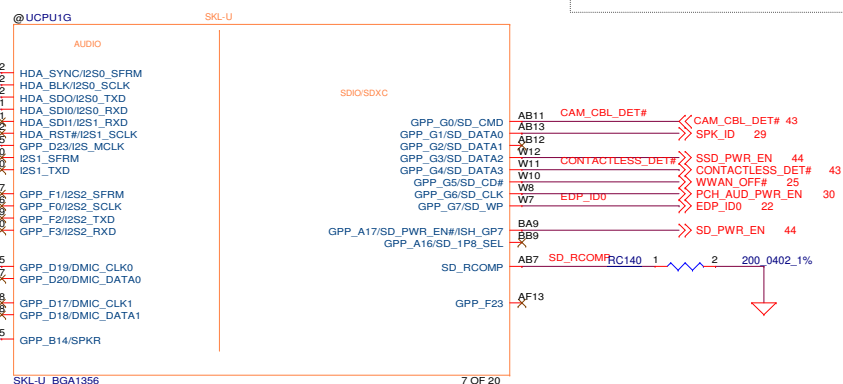
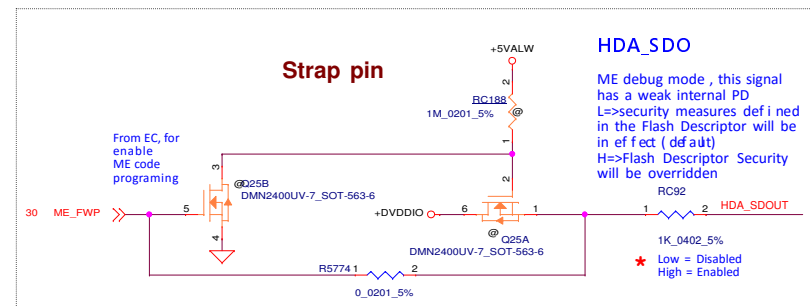
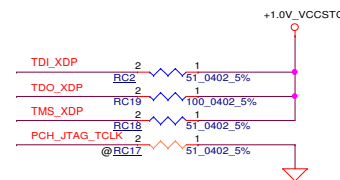
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Issued Date	2015/10/22	Deciphered Date	2013/10/28
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Title		P08-MCP(4/14)GSPI,I2C,UART,ISH	
Size	Document Number	Rev	1.0
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Date:	Tuesday, November 07, 2017	Sheet	8 of 65







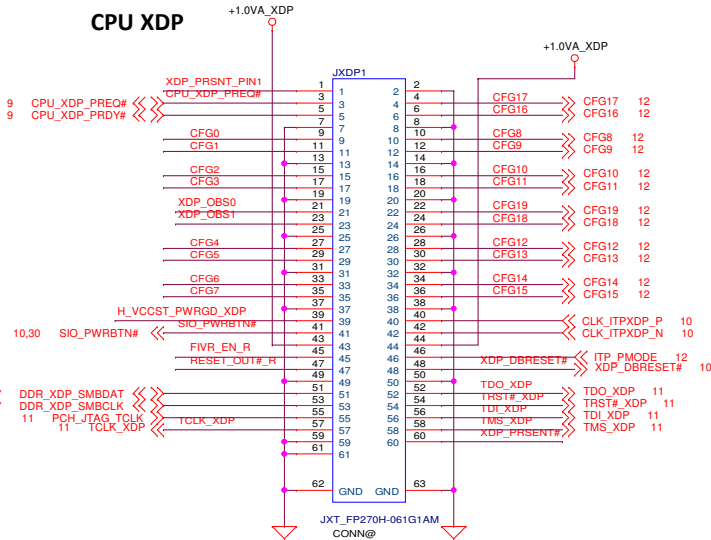
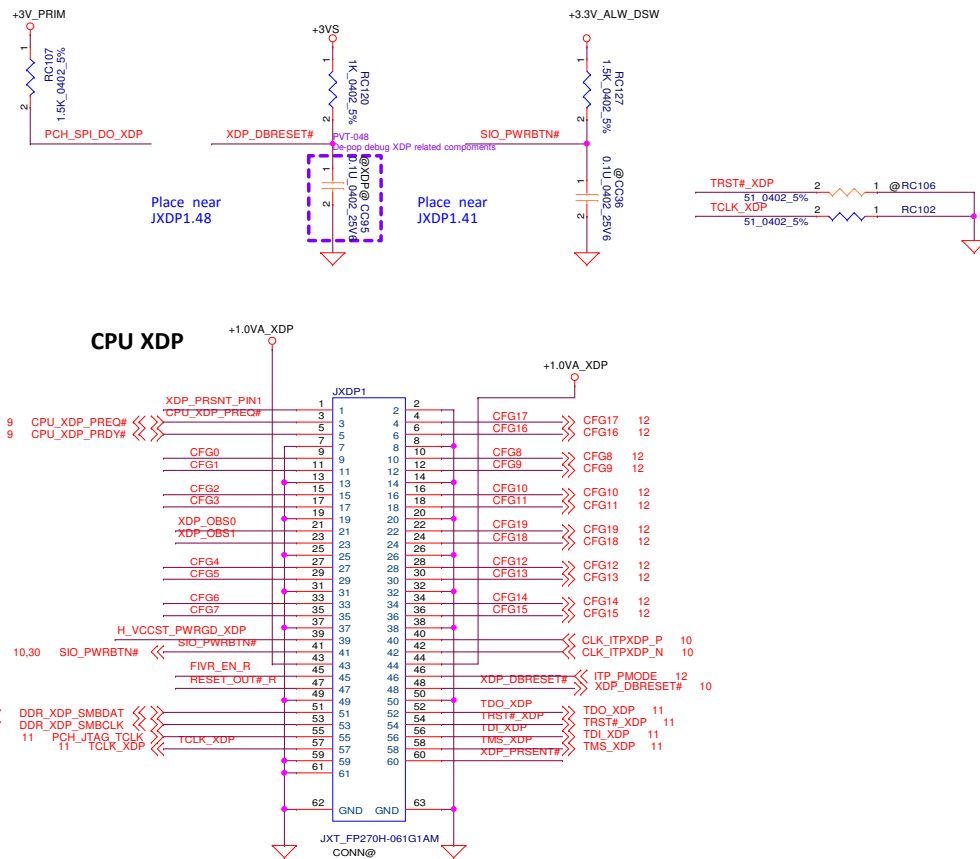


TPM_DET	
TPM	1 = W/TPM 0 = W/O TPM

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Date:	Tuesday, November 07, 2017	Sheet	11	of	65
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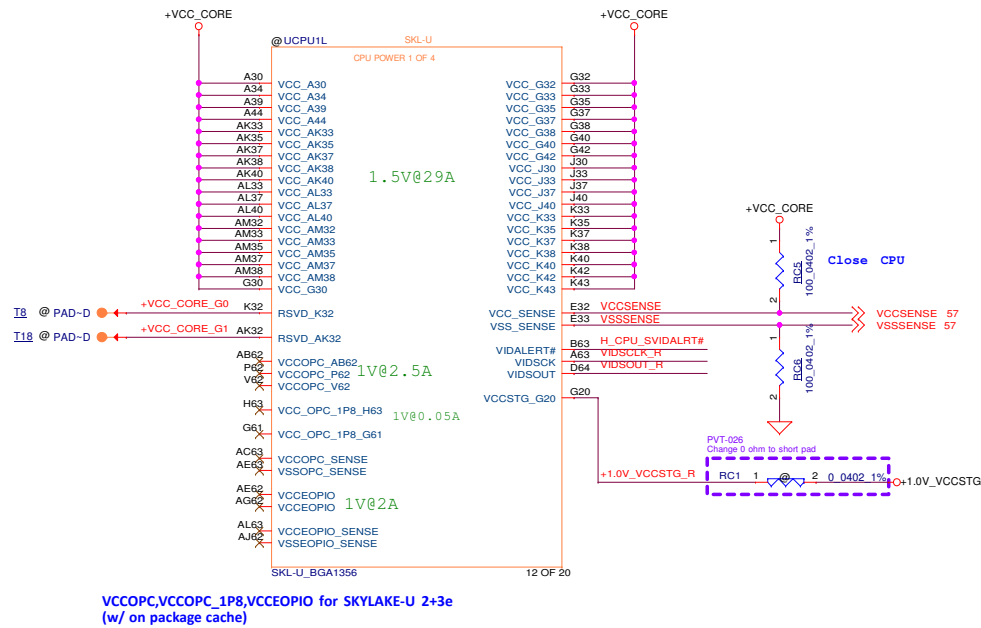


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Issued Date	2015/10/22	Deciphered Date	2013/10/28	Title	<b>P13-MCP(9/14)XDP</b>			
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PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

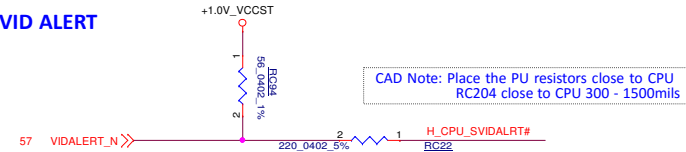
Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

**+VCC\_CORE: 0.55~1.5V, 29A**  
**+VCC\_EDRAM: 1V, 2.5A**  
**+V1.8S\_EDRAM: 1.8V, 50mA**  
**+VCC\_EOPIO: 0.8~1V, 2A**

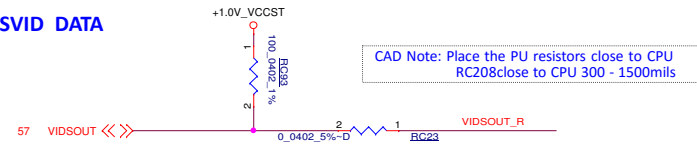


VCCOPC,VCCOPC\_1P8,VCCEPIO for SKYLAKE-U 2+3e  
(w/ on package cache)

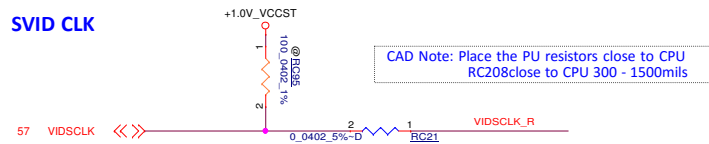
#### SVID ALERT



#### SVID DATA



#### SVID CLK



CDI#61280  
10.2.7 SVID Topology  
Table 10-9. SVID Bus Routing Guidelines  
need double pull high

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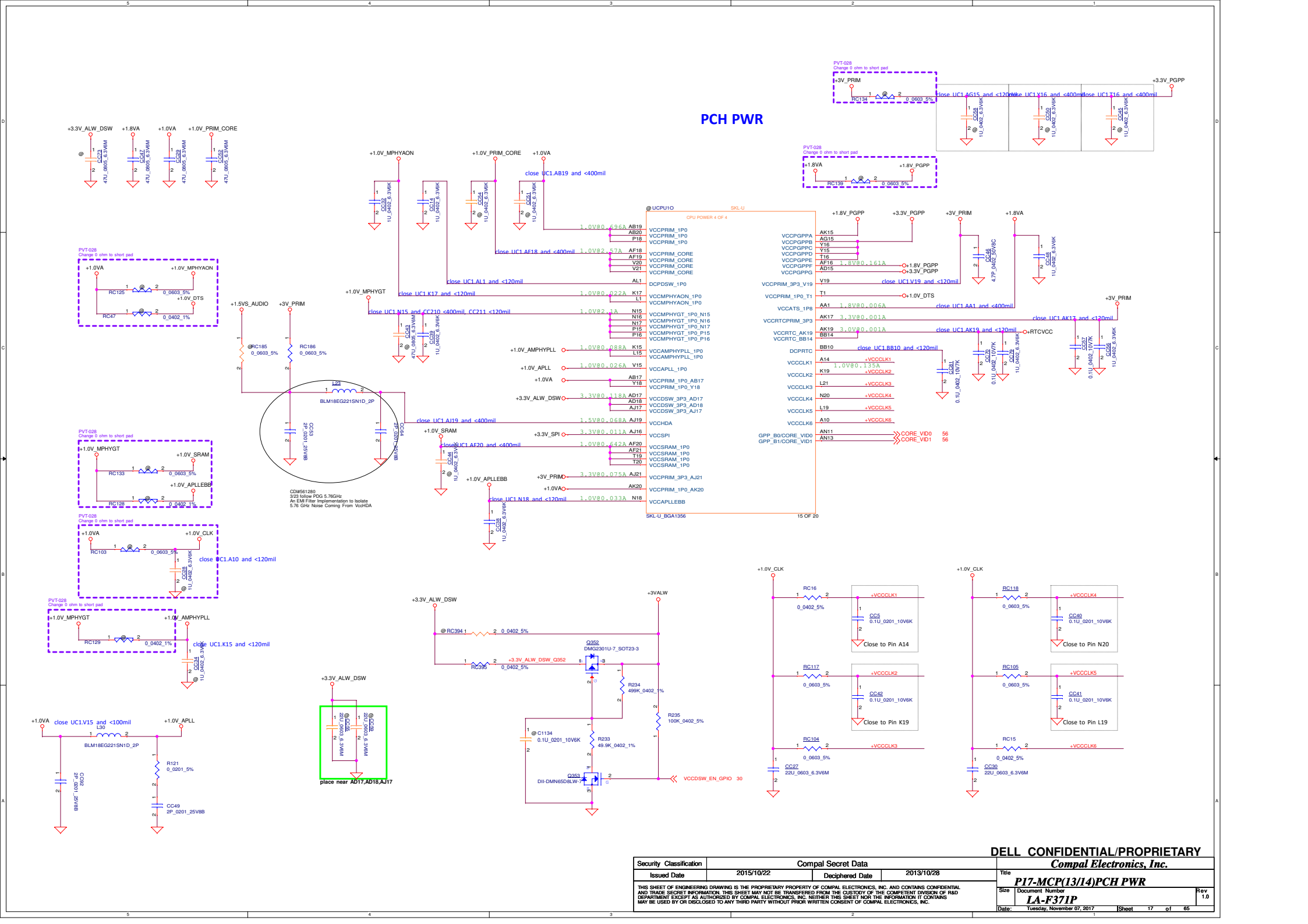
Security Classification	Compal Secret Data			Title		
Issued Date	2015/10/22	Deciphered Date	2013/10/28	P14-MCP(10/14)PWR-VCC CORE		
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					LA-F371P	1.0
				Date:	Tuesday, November 07, 2017	Sheet 14 of 65





1





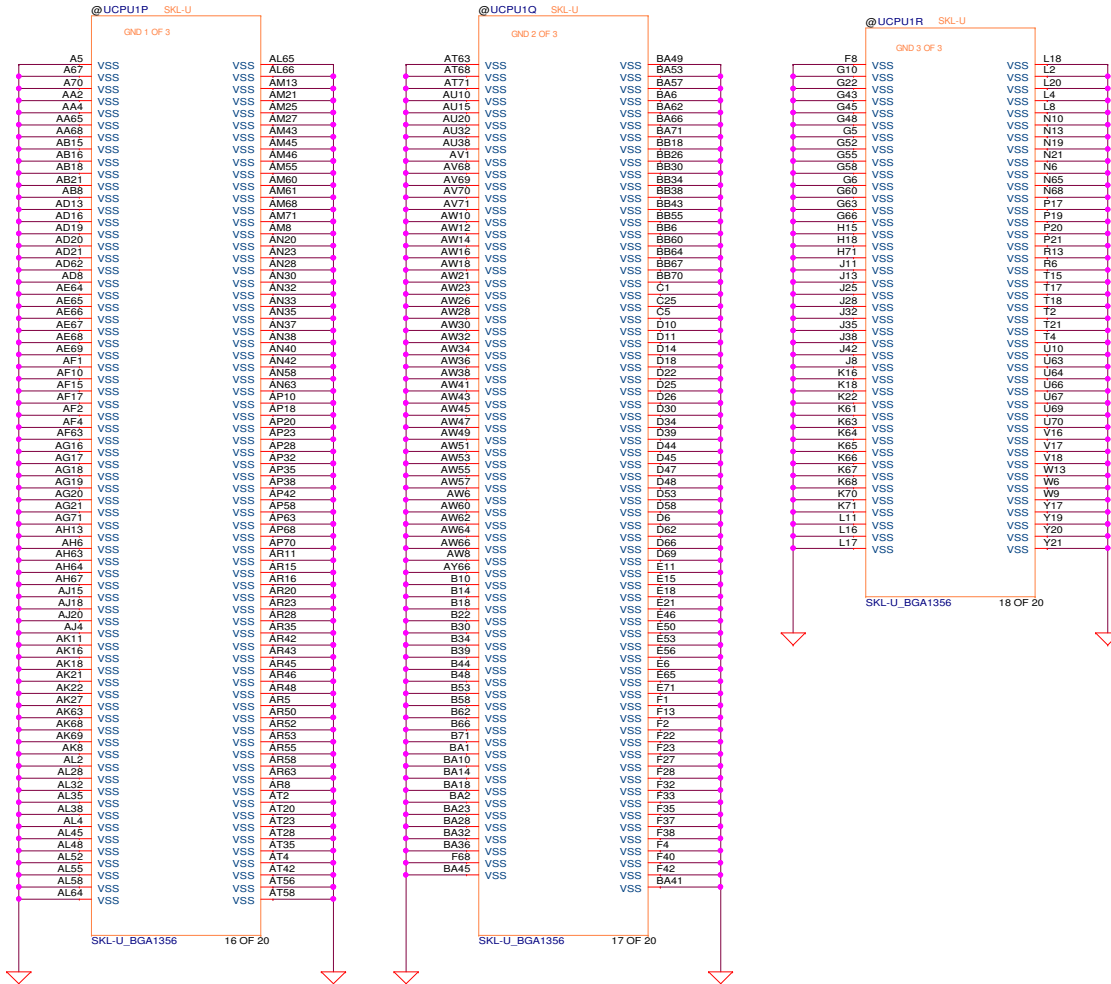
PCH PWR

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				Rev 1.0
				Date: Tuesday, November 07, 2017 Sheet 17 of 65

Note1: VCCPRIM\_CORE Implementat i on ut h PCH CORE\_V D Reco mnendat i on

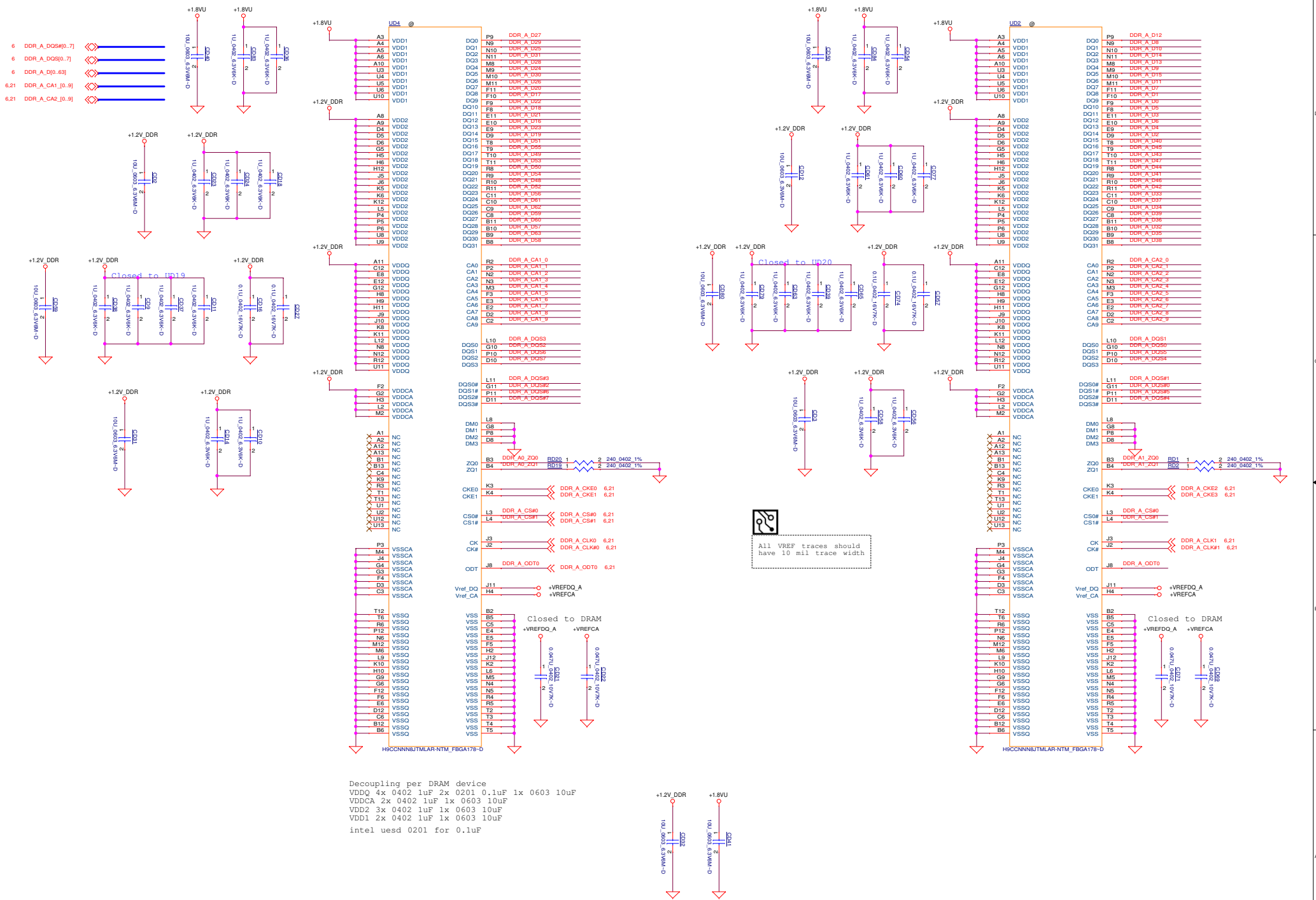
R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



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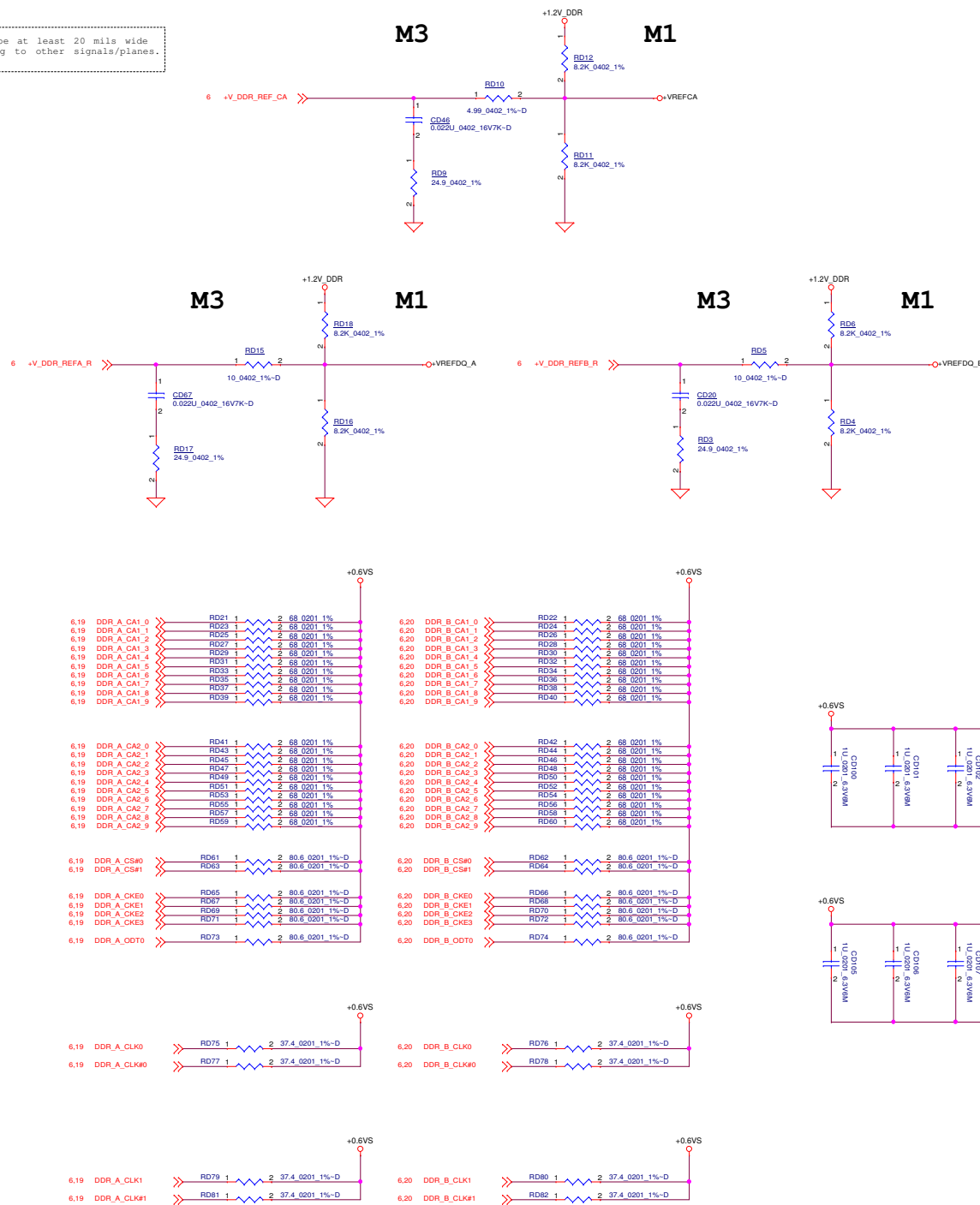
Decoupling per DRAM device  
VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF  
VDDCA 2x 0402 1uF 1x 0603 10uF  
VDD2 3x 0402 1uF 1x 0603 10uF  
VDD1 2x 0402 1uF 1x 0603 10uF  
intel used 0201 for 0.1uF

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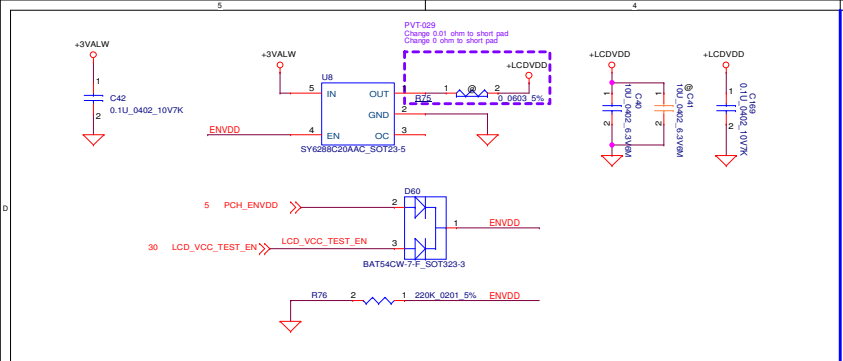




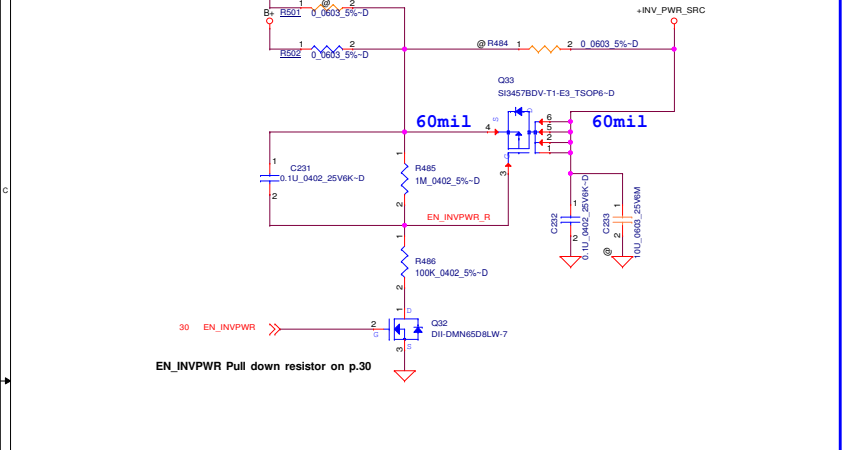
VREF traces should be at least 20 mils wide  
with 20 mils spacing to other signals/planes.



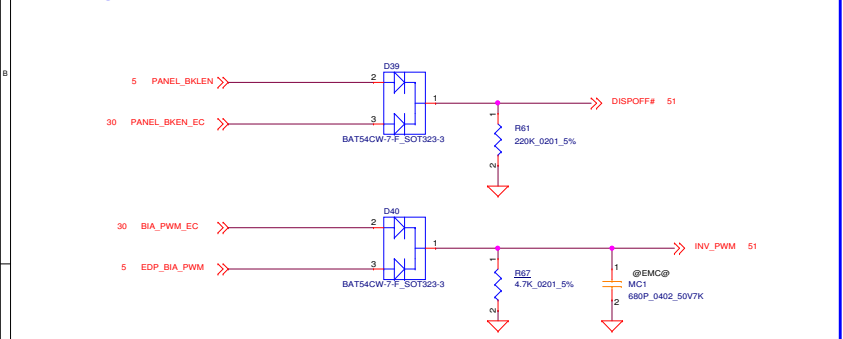
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Title		Size		Document Number	
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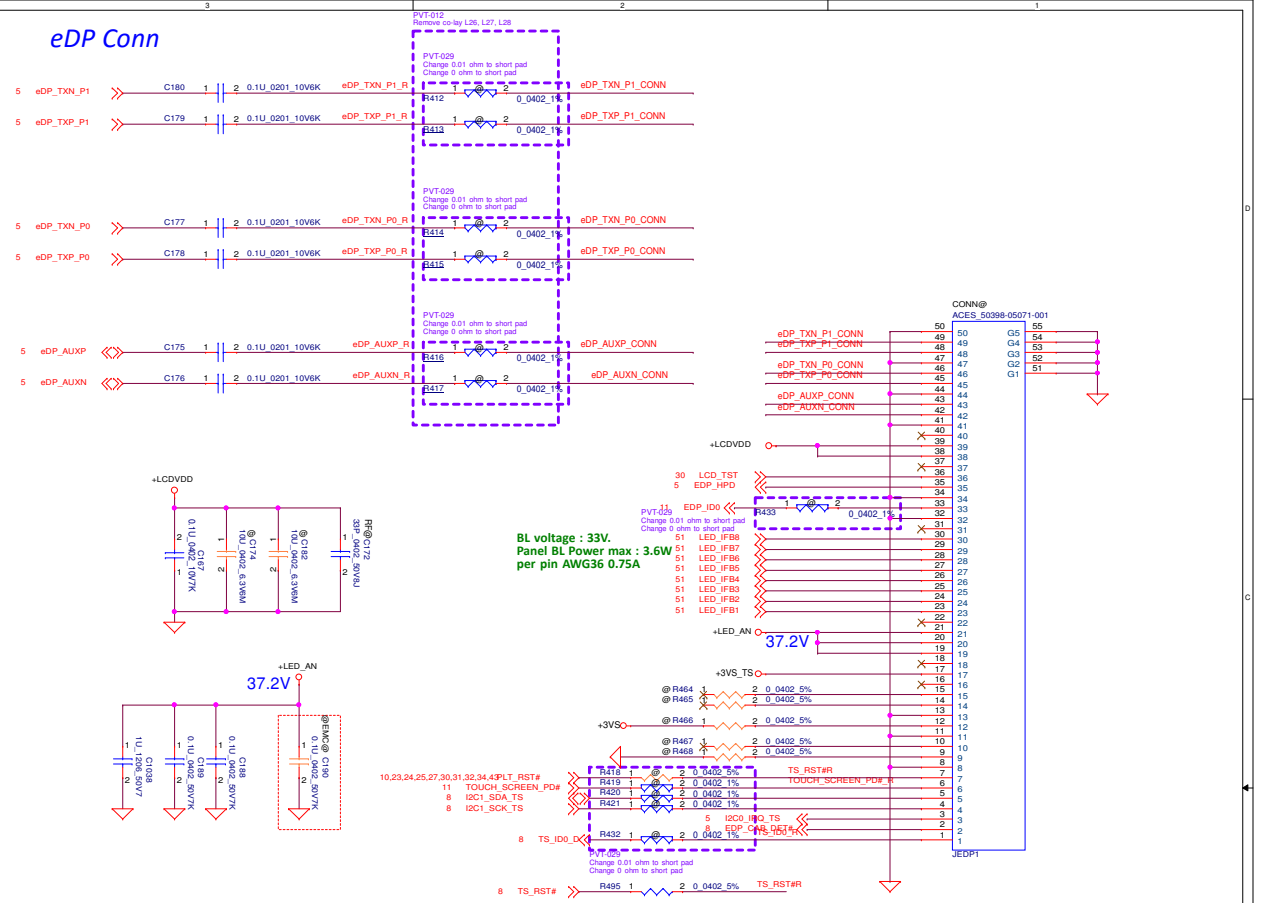
## eDP BackLight Power



## BackLight PWM Control

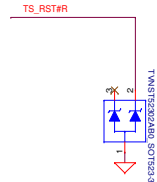
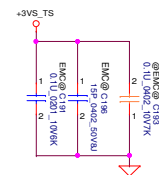


## eDP Conn



## Truth Table for EDP\_ID/TS\_ID0

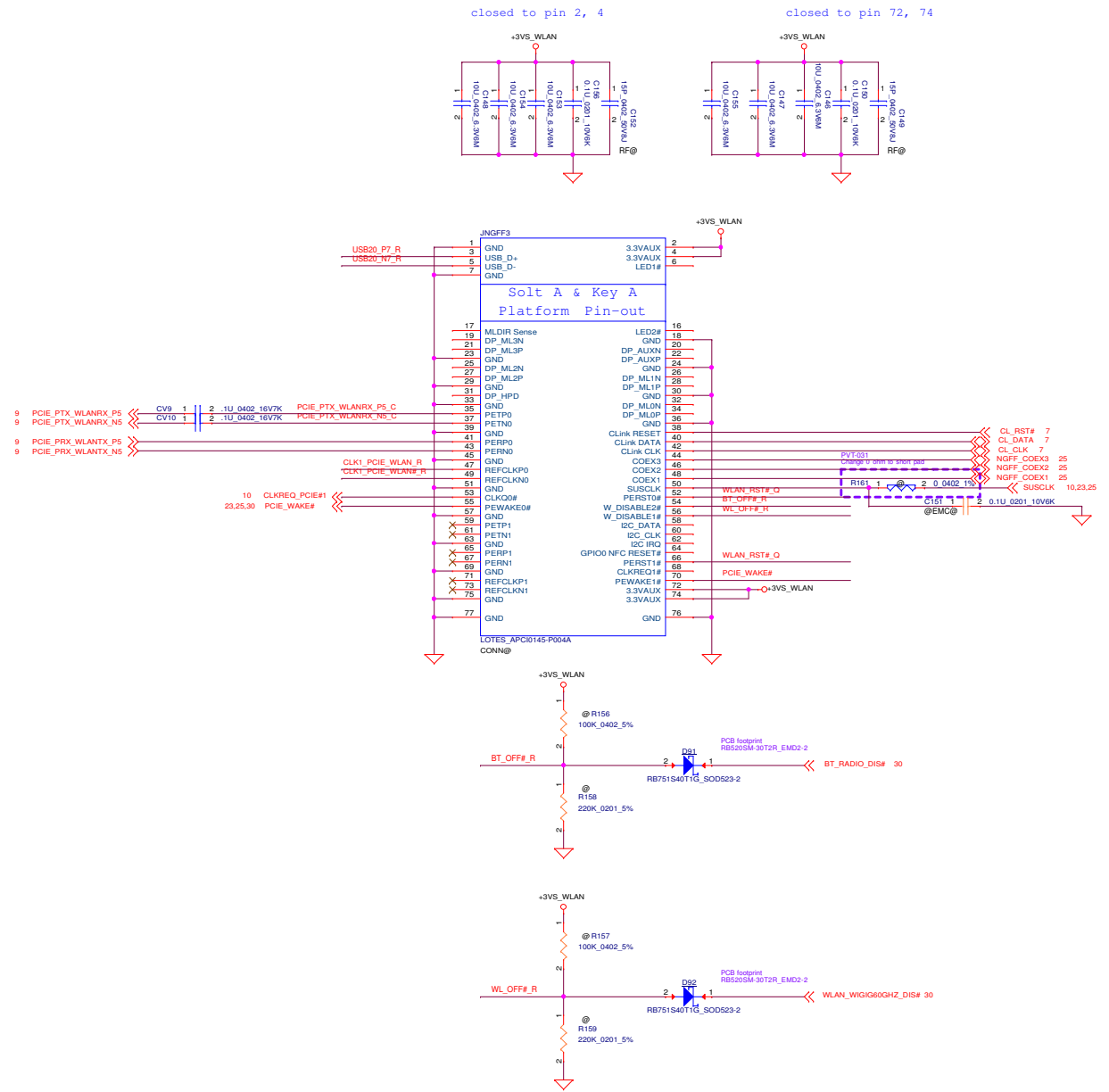
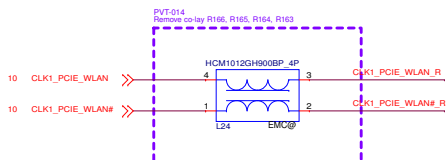
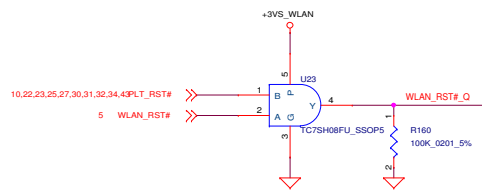
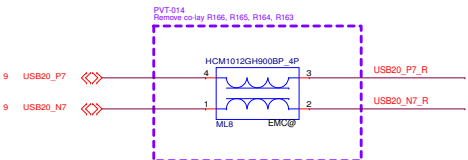
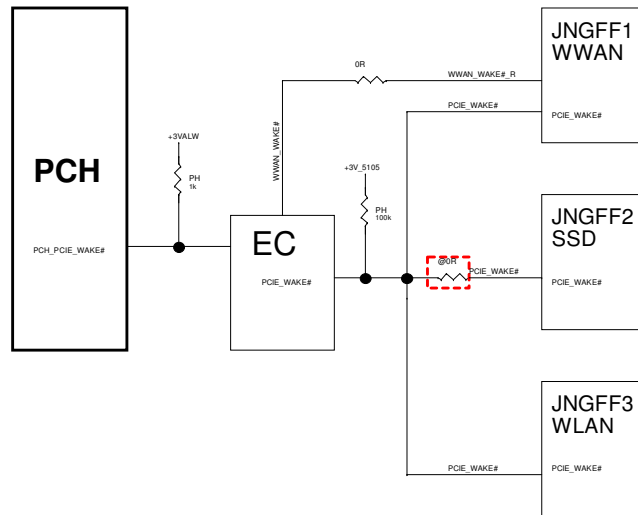
Touch Controller	Panel	EDP_ID0	TS_ID0
TPK	SHARP	LOW	LOW
Laibao	SHARP	LOW	High
HH	BOE	High	LOW
Reserved		High	High



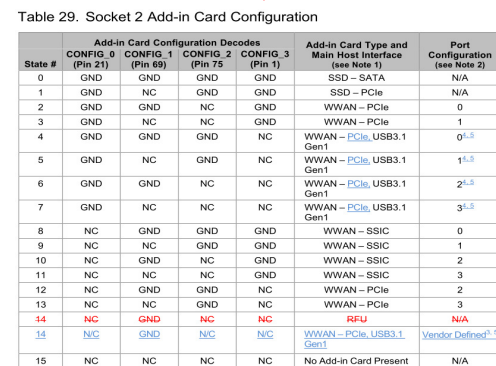
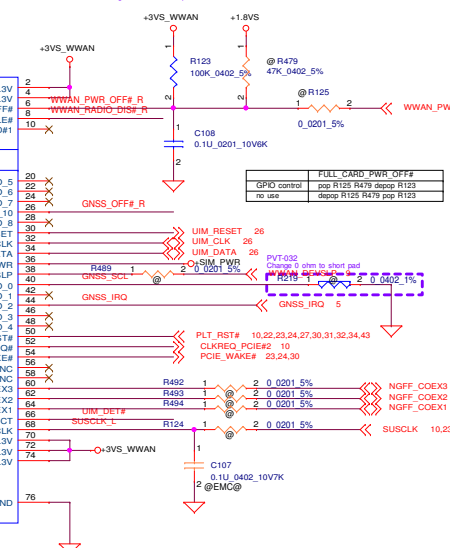
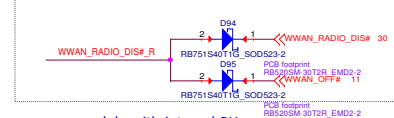




# Wireless LAN



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				Date: Tuesday, November 07, 2017
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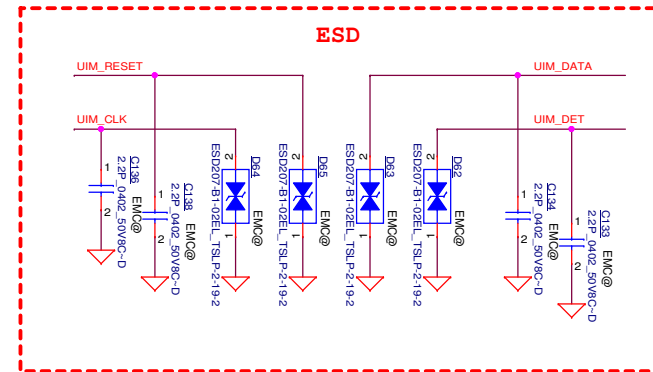
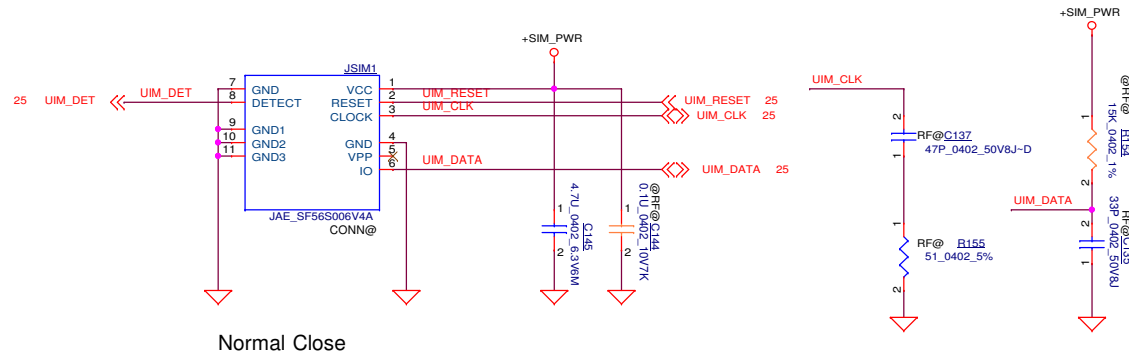


Add-In Card Configuration Decodes					Add-In Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
State #	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	NC	NC	NC	NC	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – PCIe, USB3.1 Gen1	0 <sup>1,5</sup>
5	GND	NC	GND	NC	WWAN – PCIe, USB3.1 Gen1	1 <sup>1,5</sup>
6	GND	GND	NC	NC	WWAN – PCIe, USB3.1 Gen1	2 <sup>1,5</sup>
7	GND	NC	NC	NC	WWAN – PCIe, USB3.1 Gen1	3 <sup>1,5</sup>
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	NC	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
14	NC	GND	NC	NC	RFU	N/A
15	NC	GND	NC	NC	WWAN – PCIe, USB3.1 Gen1	Vendor Defined <sup>1</sup>
16	NC	NC	NC	NC	No Add-In Card Present	N/A

Enable PCIe and USB 3.1 Gen1 on M.2 Card Key B  
spec. ECN updated on 2017/02/10

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# uSIM CONN



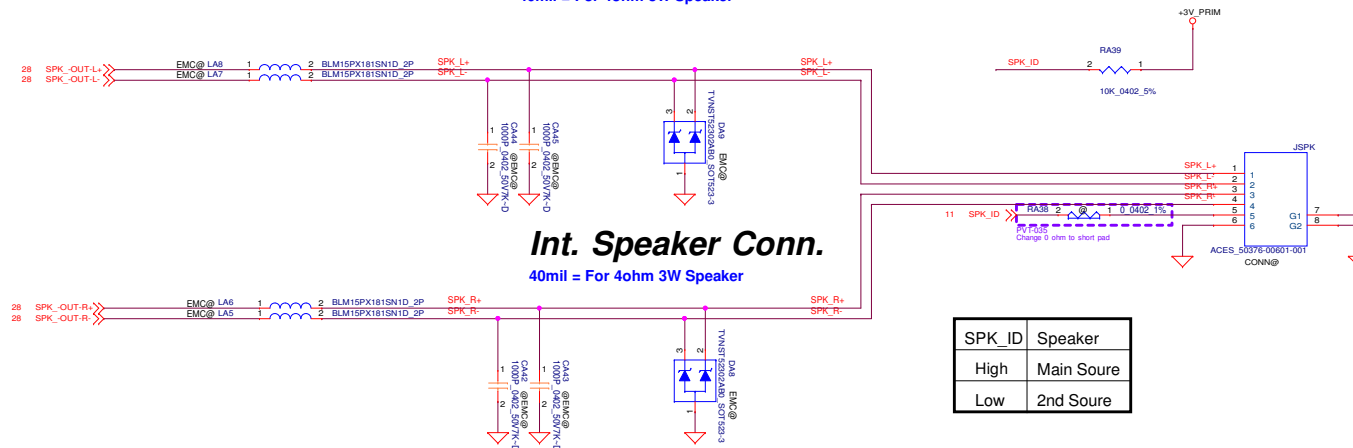
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				Size	Document Number
				LA-F371P	
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				Sheet	26 of 65
				Rev	1.0



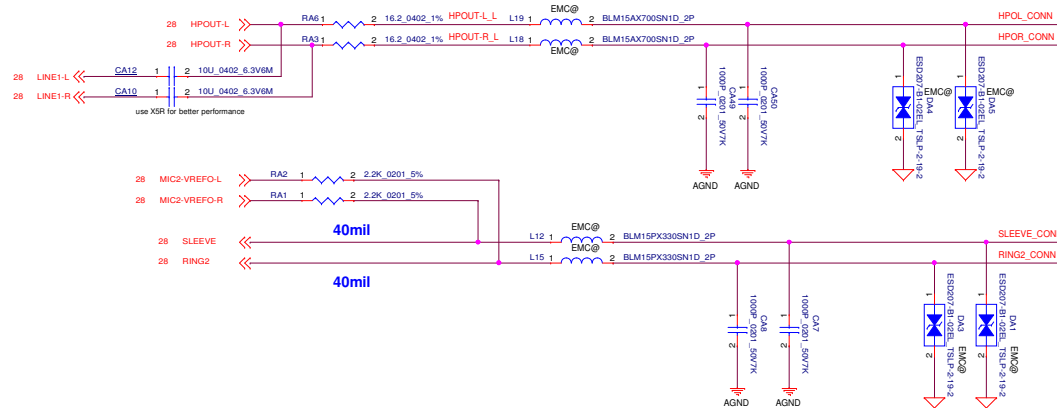


## Int. Speaker Conn.

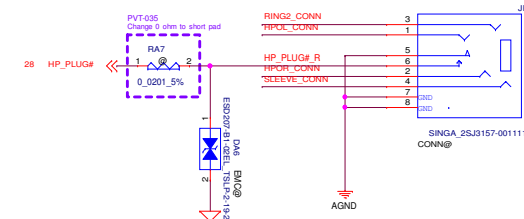
40mil = For 4ohm 3W Speaker



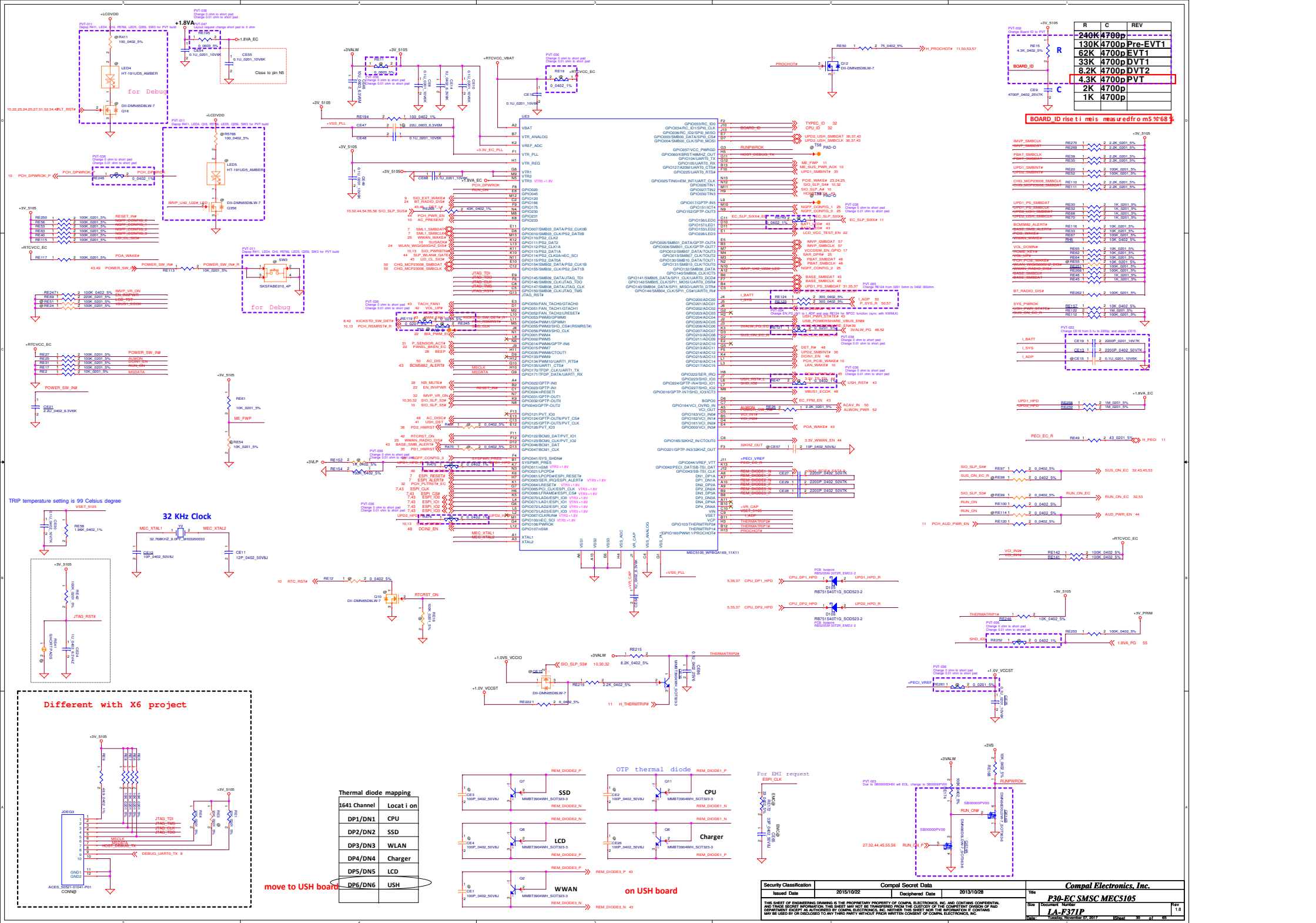
## Universal Audio Jack



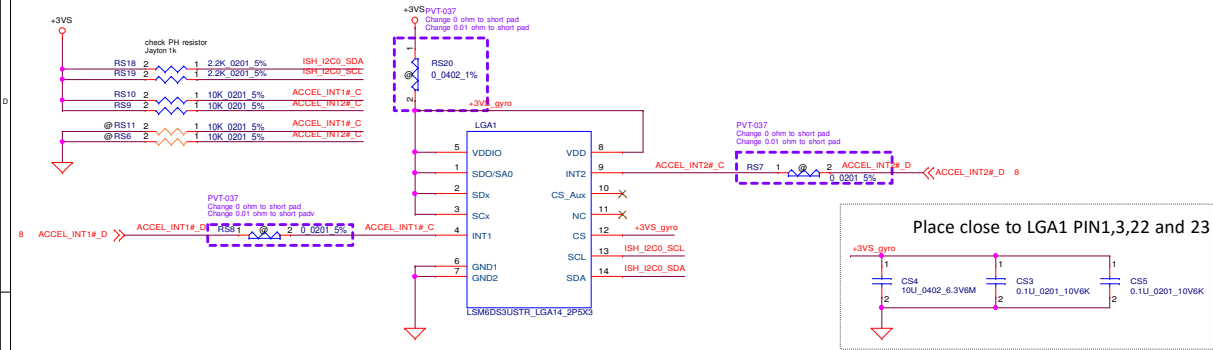
## Universal Audio Jack CONN





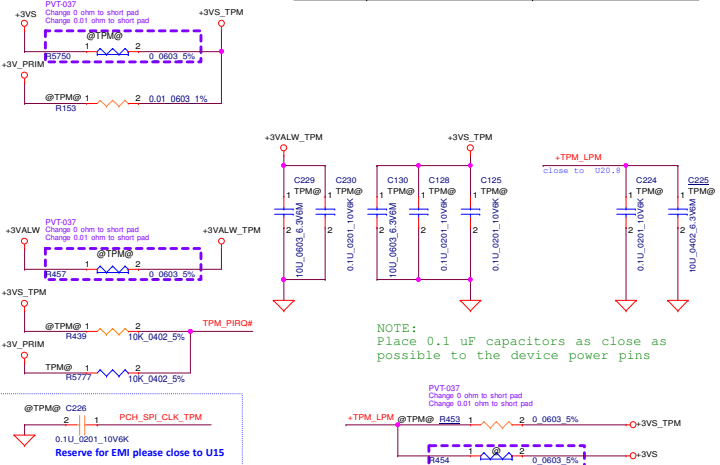


Gyro + Accelerometer

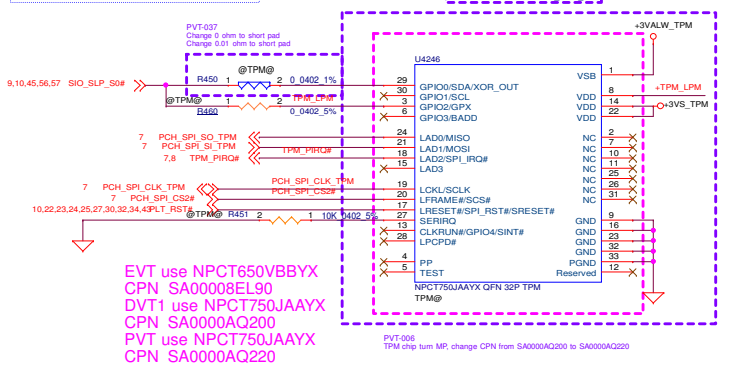
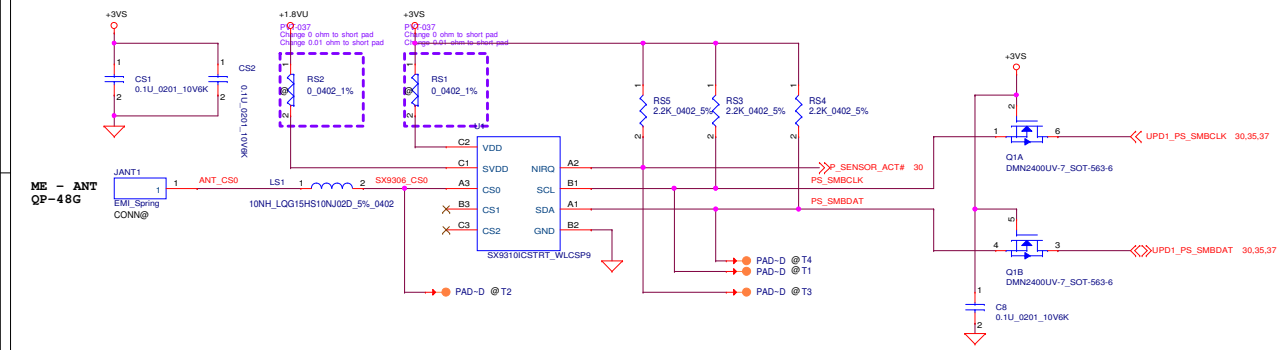


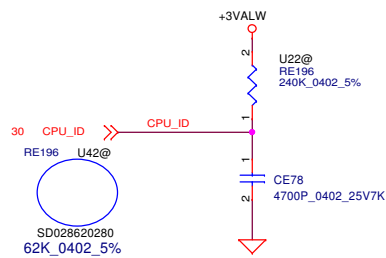
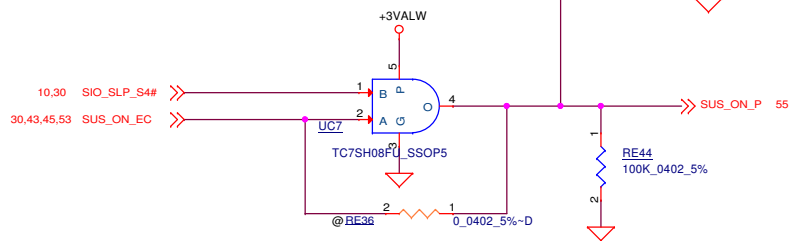
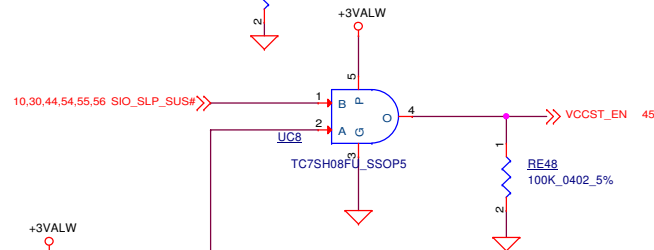
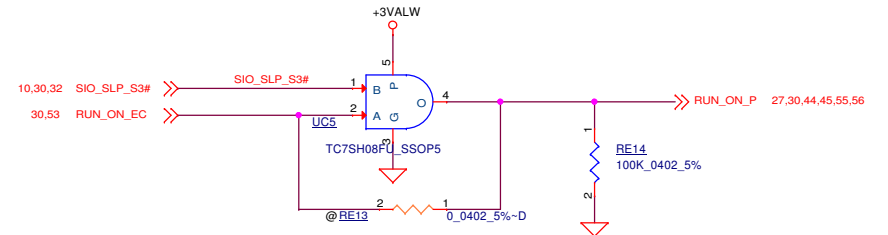
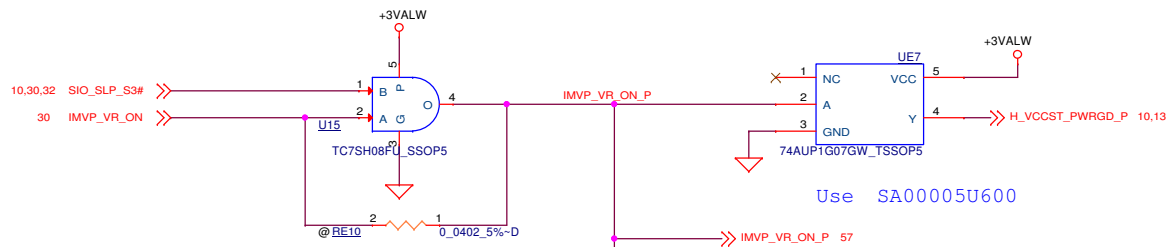
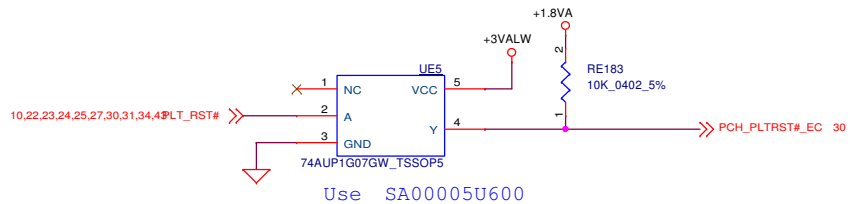
TPM

	Pop	De-pop
NPCT65x	R153, R451, R460	R5750, R450
NPCT75x	R5750, R450	R153, R451, R460

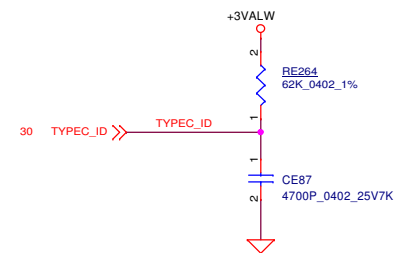


SAR Proximity Sensor



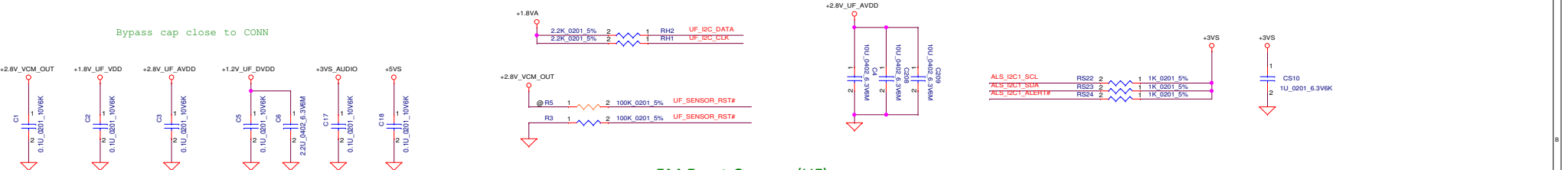
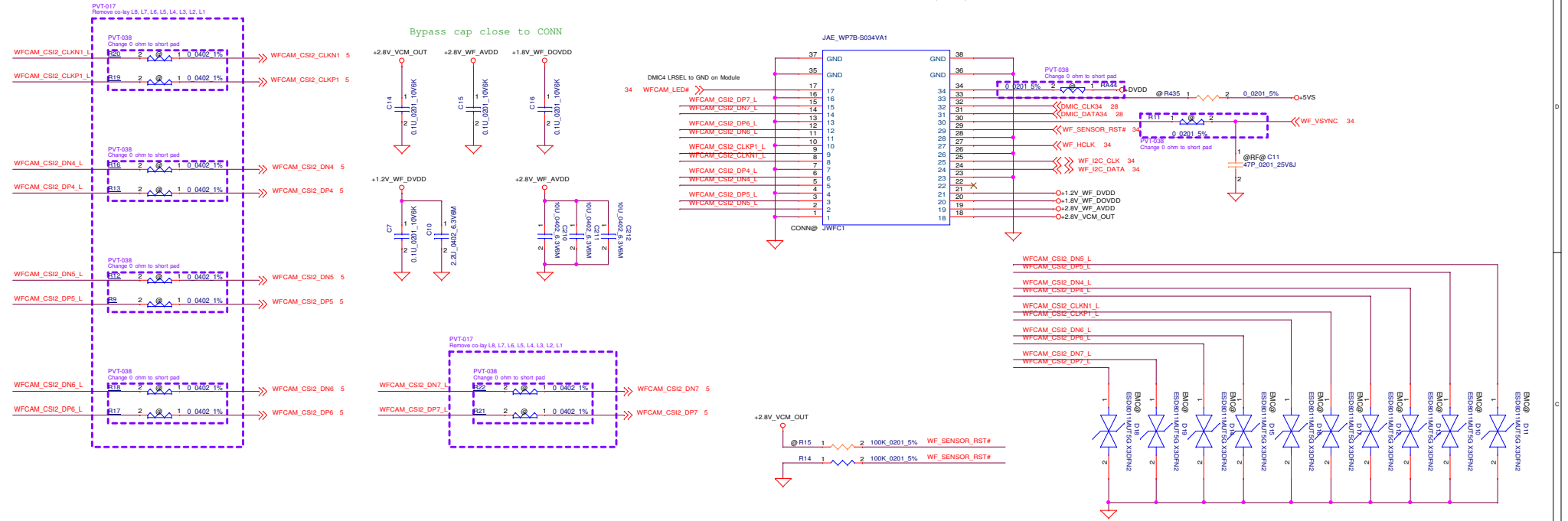


RE196	CE78	REV
240K	4700p	U2+2
130K	4700p	
62K	4700p	U4+2
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

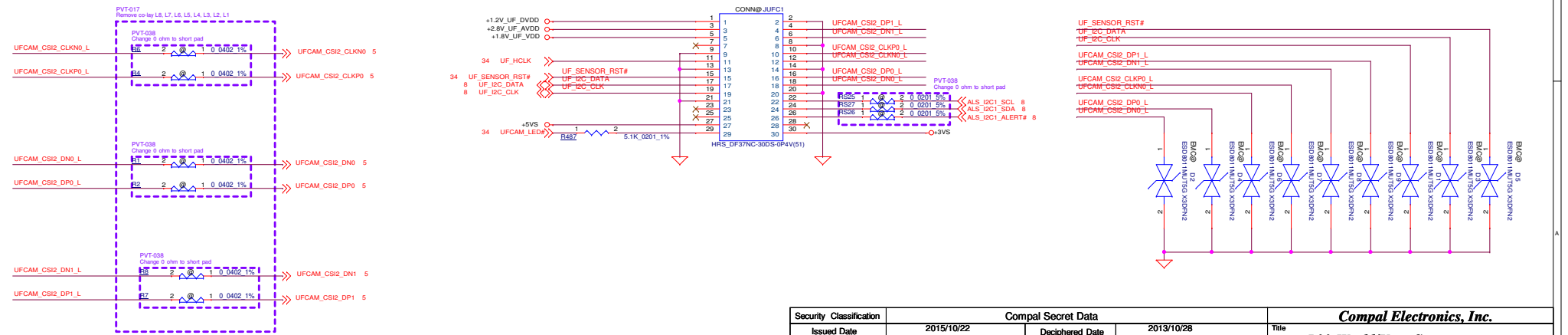


RE264	CE87	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/ AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/ AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

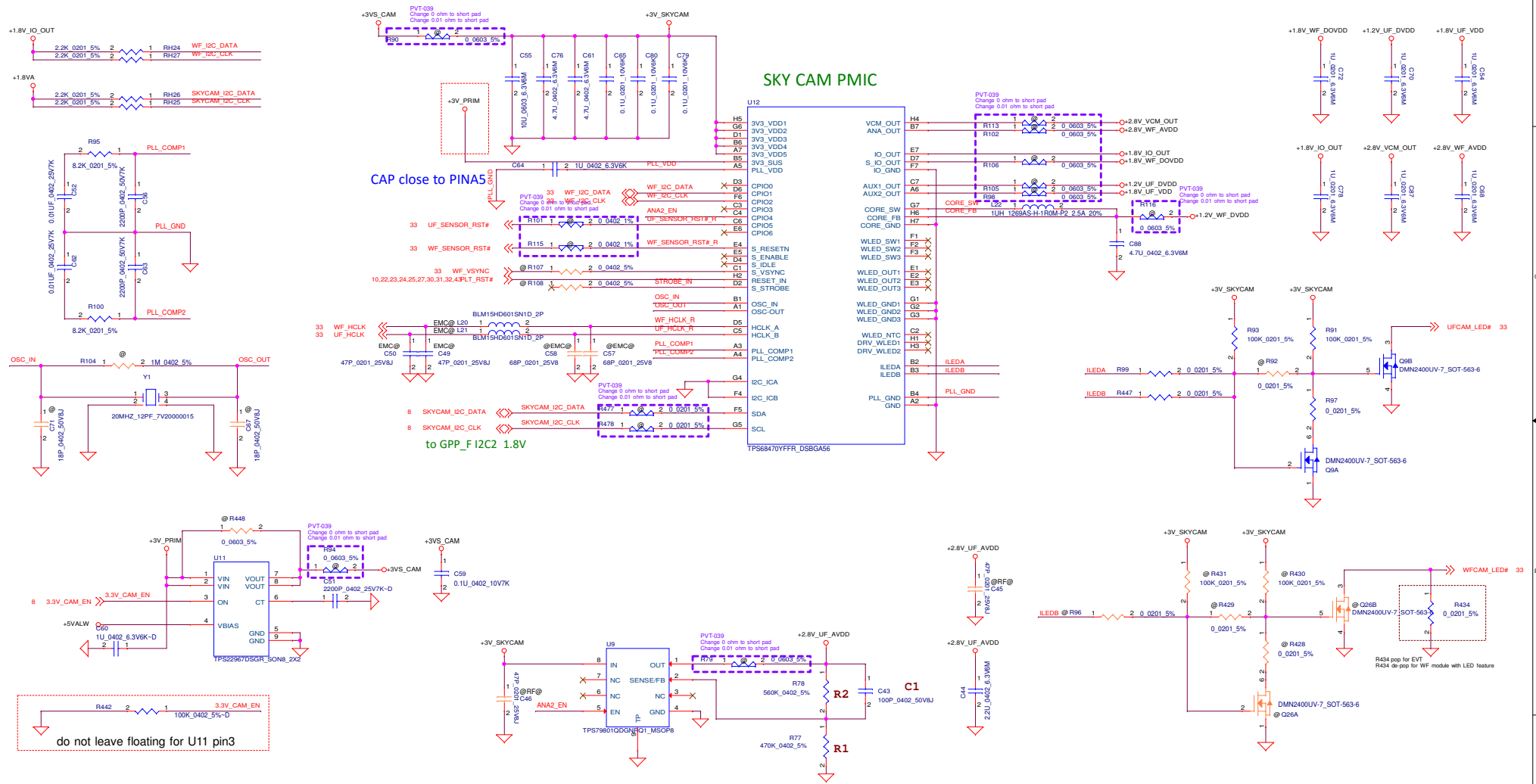
## 8M Rear Camera (WF)



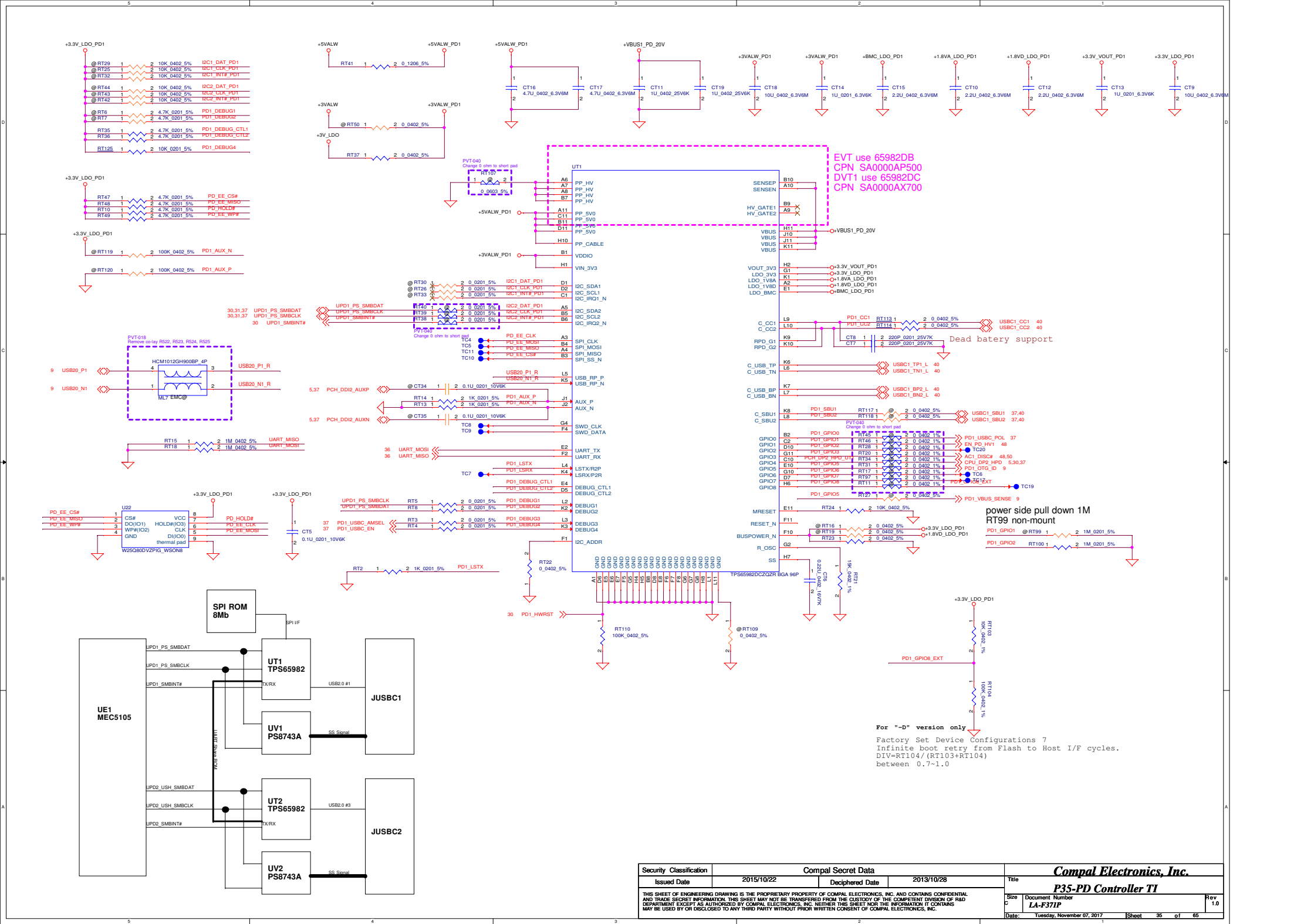
## 5M Front Camera (UF) DF37NC-30DS-0.4V(51)



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				Document Number
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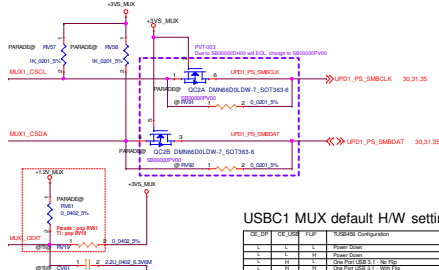
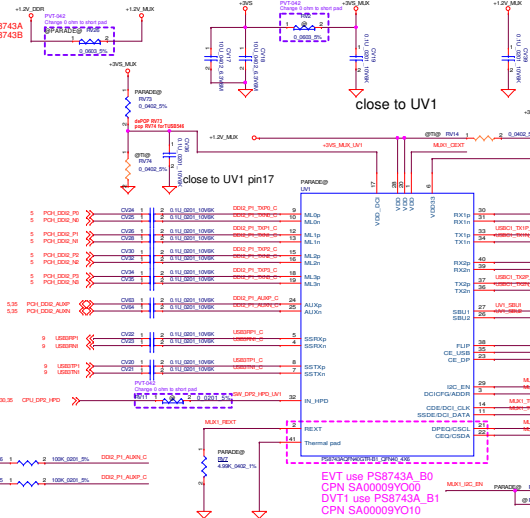
$V_{OUT} = 1.275 \text{ V} (1 + R2 / R1) + I_{FB} * R2$   
 $V_{FB} = 1.275 \text{ V}$   
 $I_{FB} = 0.53 \mu\text{A at } 25^\circ\text{C}$   
**Output Range = 1.275 V to 28 V**  
  
**A 100-pF capacitor (C1) placed in parallel with R2 of the output divider is necessary**





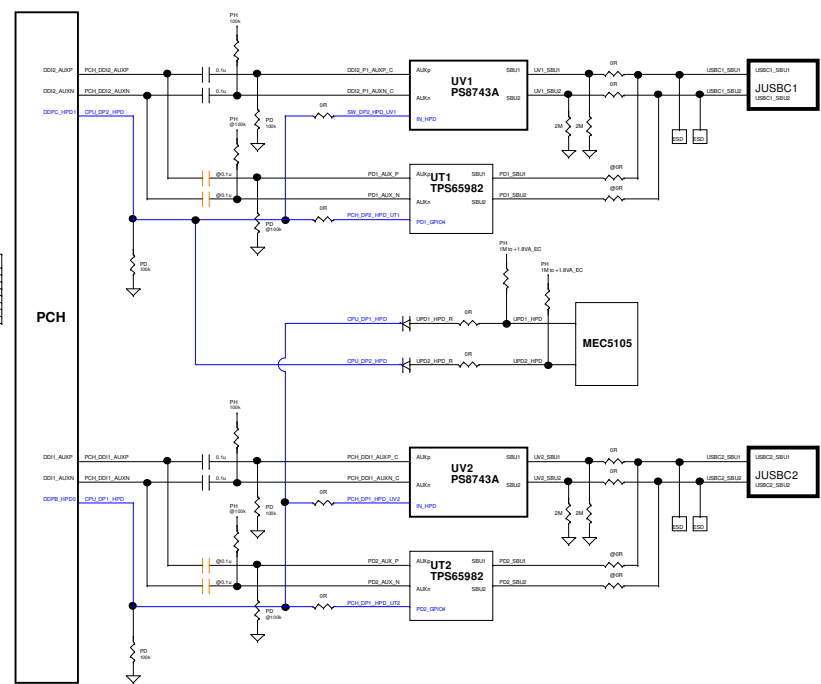
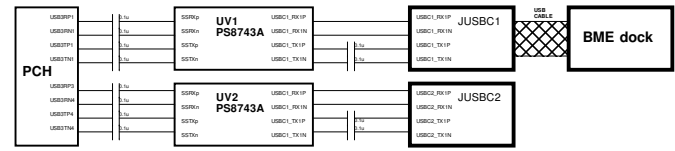


RV26 pop and RV14 de-pop for PS8743A  
RV26 de-pop and RV14 pop for PS8743B



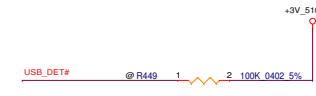
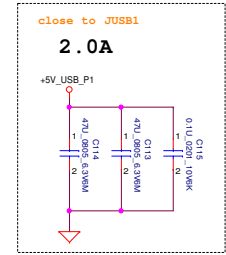
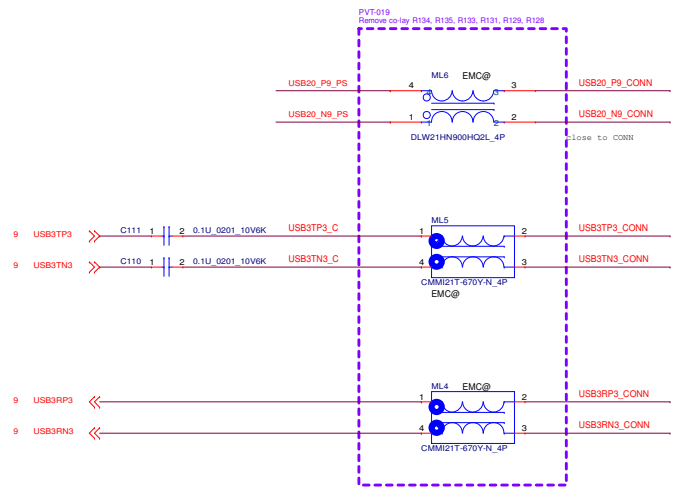
USB1 MUX default H/W setting									
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2	2	2	2	2	2	2	2	2	2
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4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6
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9	9	9	9	9	9	9	9	9	9
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### USB 3.0 AC Coupling Capacitor Topology



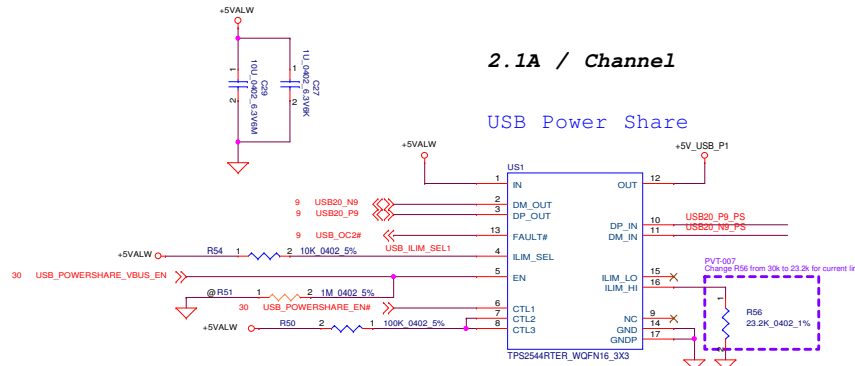
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				Checked	
				Released	





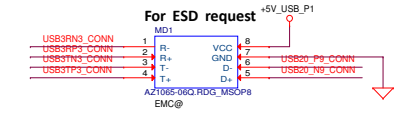
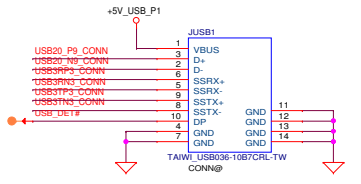
## 2.1A / Channel

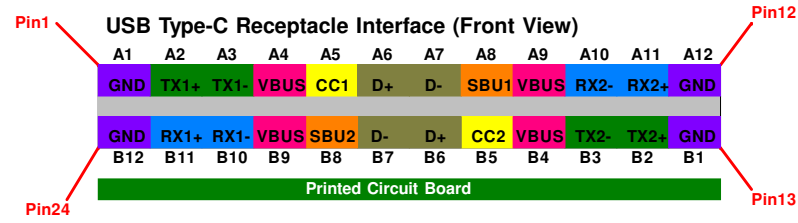
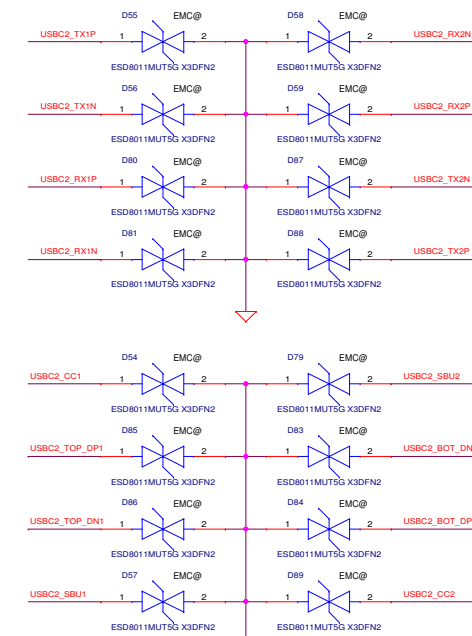
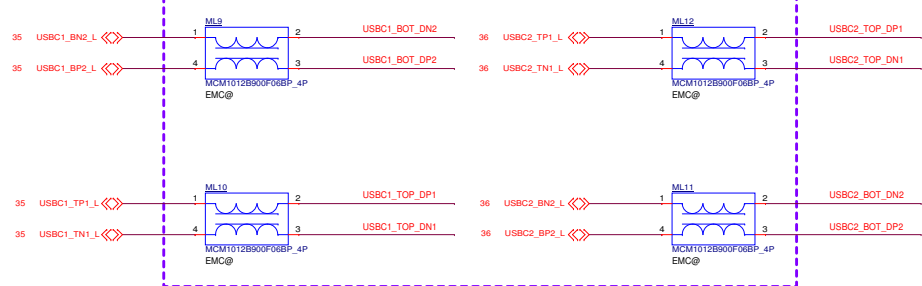
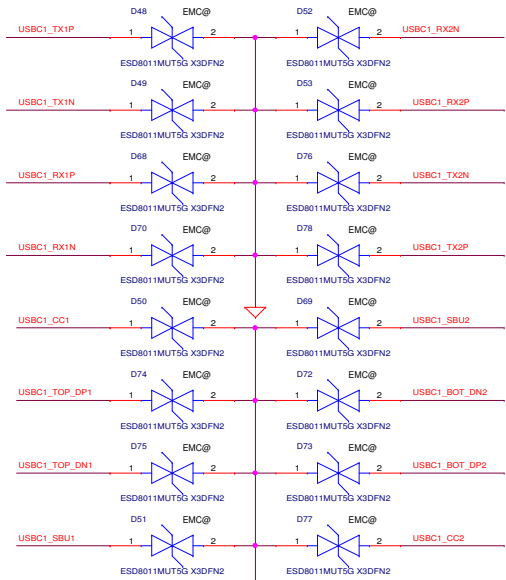
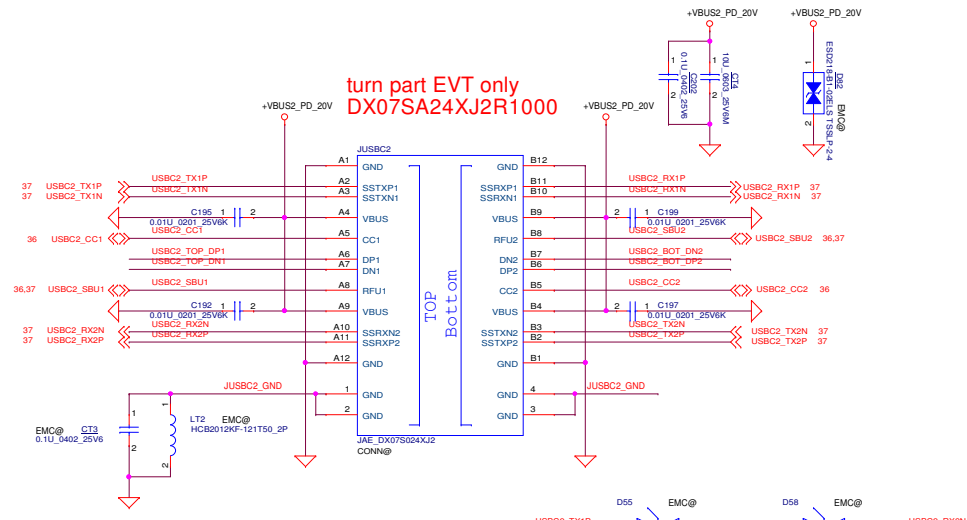
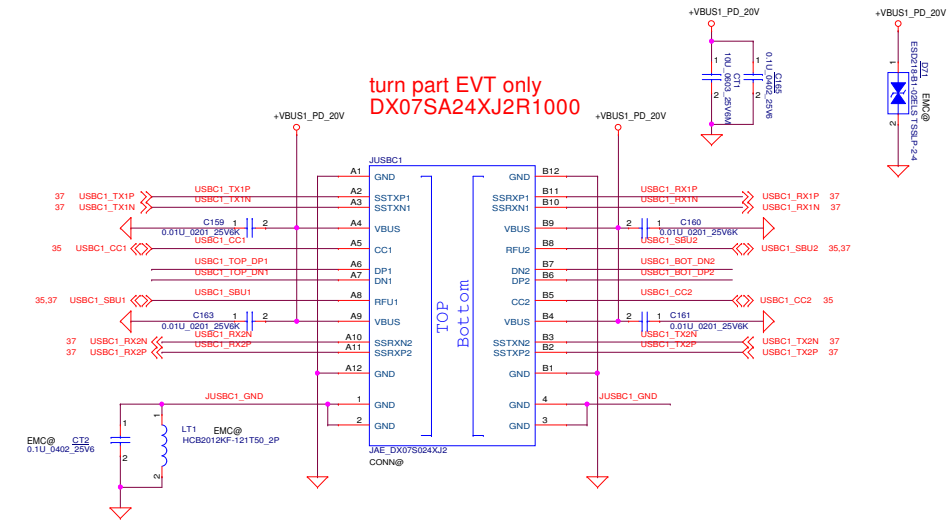
### USB Power Share



CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

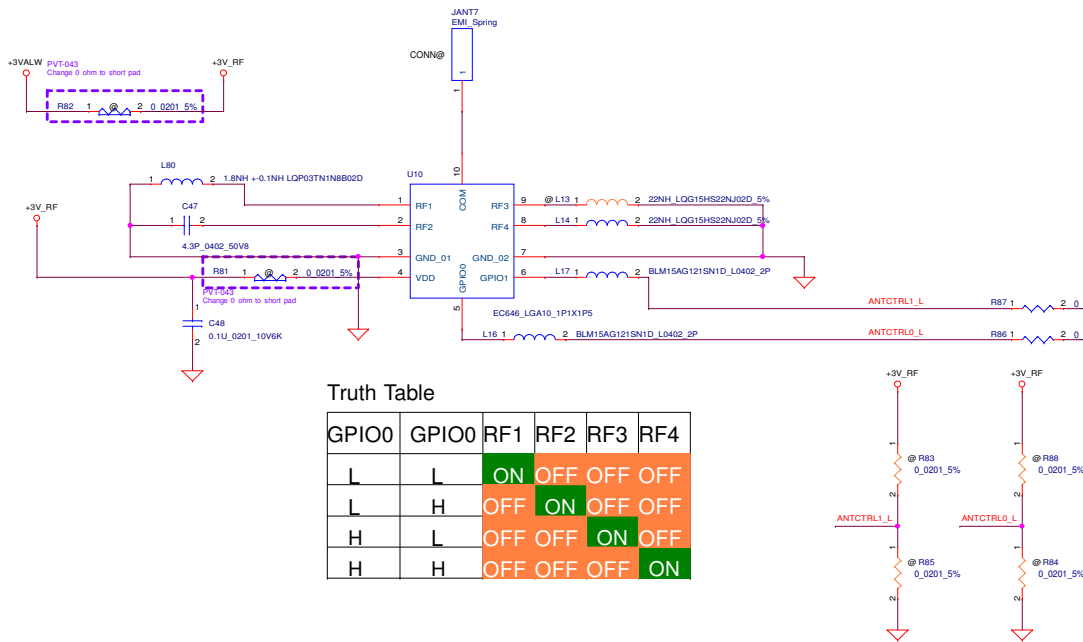
### USB TYPE-A CONN





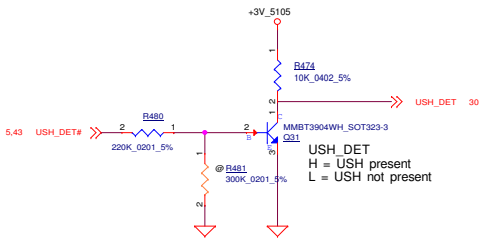
Tunable IC

RF conn for WWAN

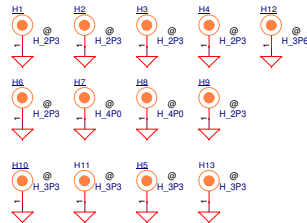
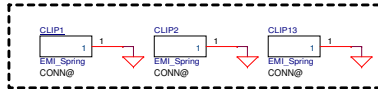
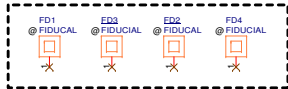


Truth Table

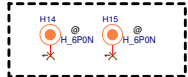
GPIO0	GPIO0	RF1	RF2	RF3	RF4
L	L	ON	OFF	OFF	OFF
L	H	OFF	ON	OFF	OFF
H	L	OFF	OFF	ON	OFF
H	H	OFF	OFF	OFF	ON



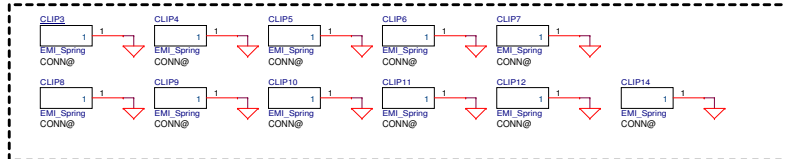
## SCREW HOLE



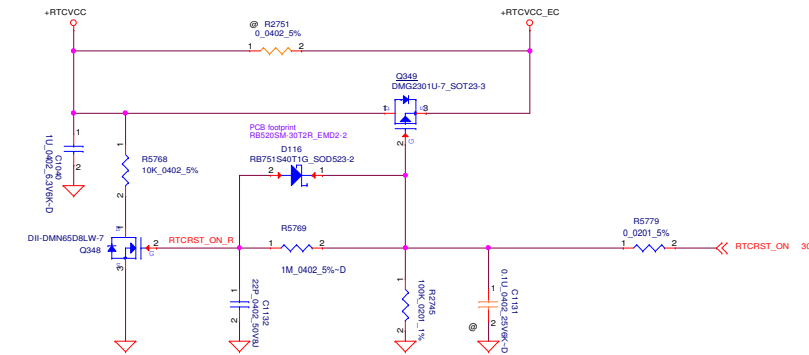
for cable routing



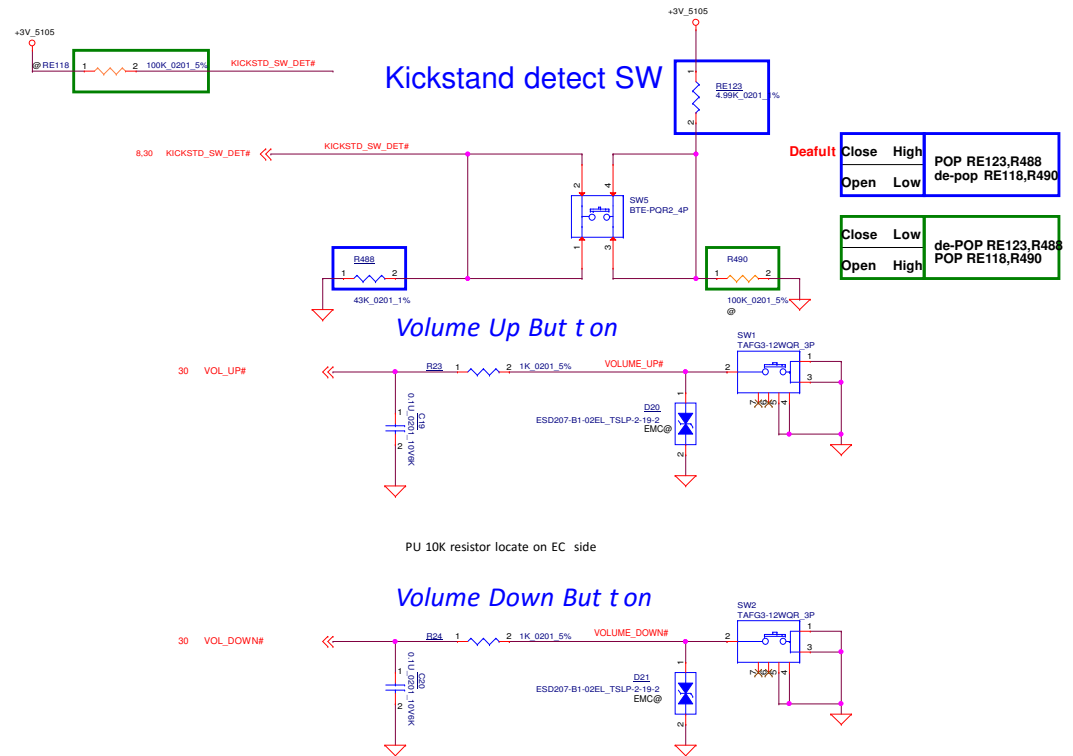
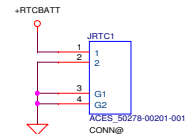
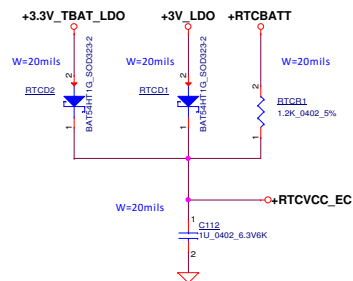
for WLAN/WWAN



for M.2 SSD/WLAN/WWAN shielding clip



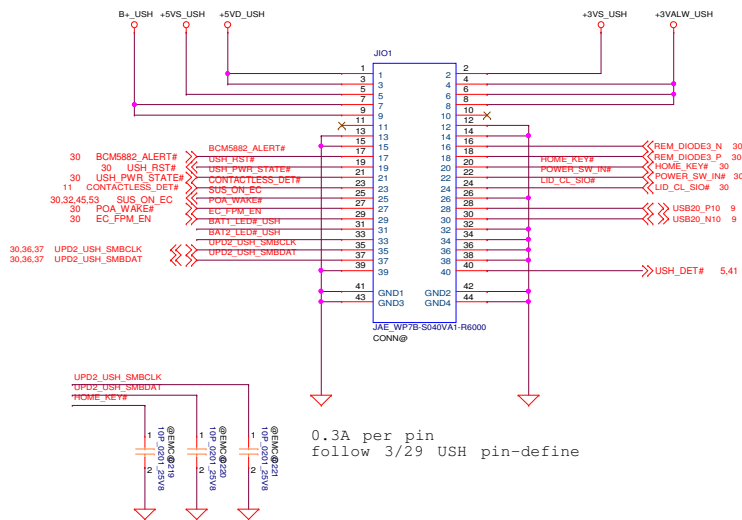
## RTC



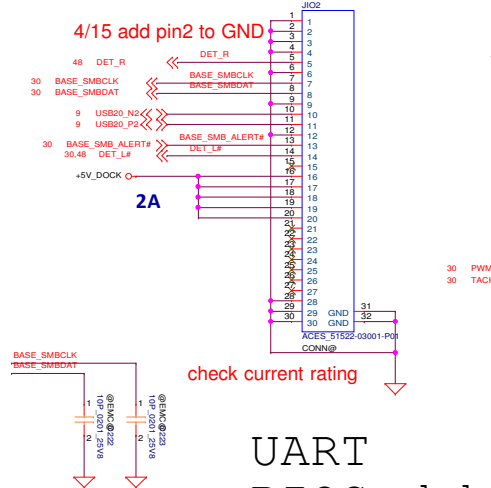
## SATA LED

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				Date:	Tuesday, November 07, 2017
				Sheet	42 of 65

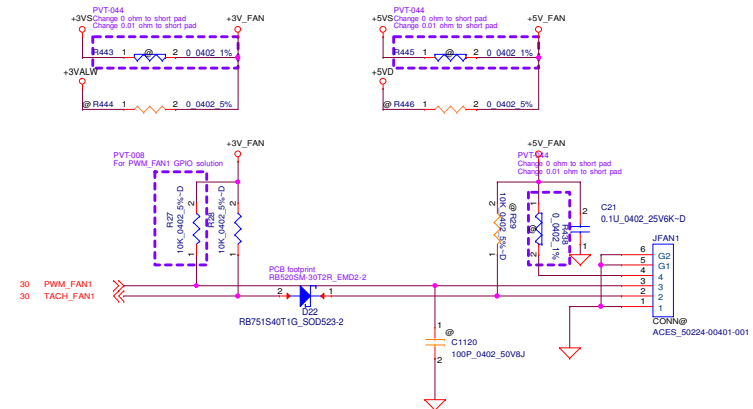
## USH CONN



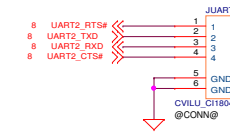
Docking CONN



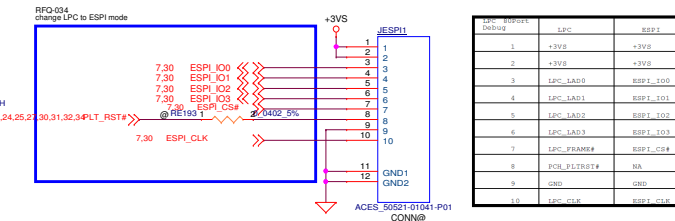
## FAN CONN



```
UART
BIOS  debug
```

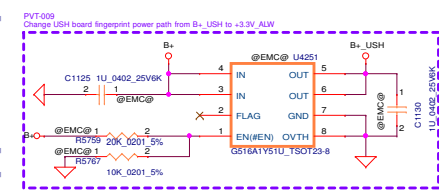
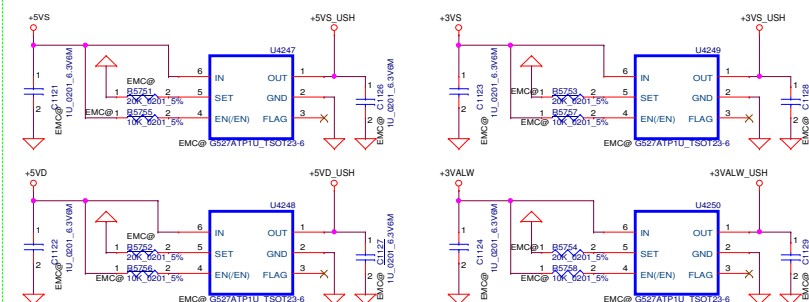
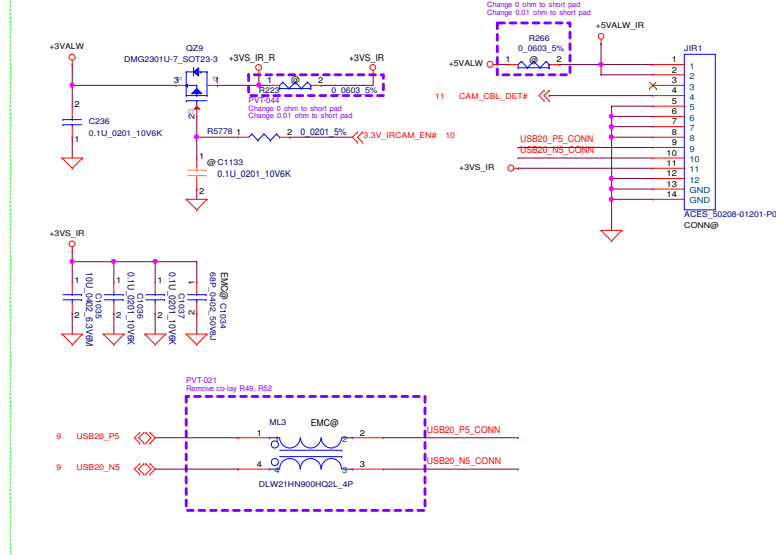


```
ESPI
BIOS debug
```



LPC Event Debug	LPC	ESP1
1	+VVS	+VVS
2	+VVS	+VVS
3	LPC_LAD0	ESP1_100
4	LPC_LAD1	ESP1_101
5	LPC_LAD2	ESP1_102
6	LPC_LAD3	ESP1_103
7	LPC_FRAME#	ESP1_CS#
8	PCB_PLTRST#	NA
9	GND	GND
10	LPC_CLK	ESP1_CLK

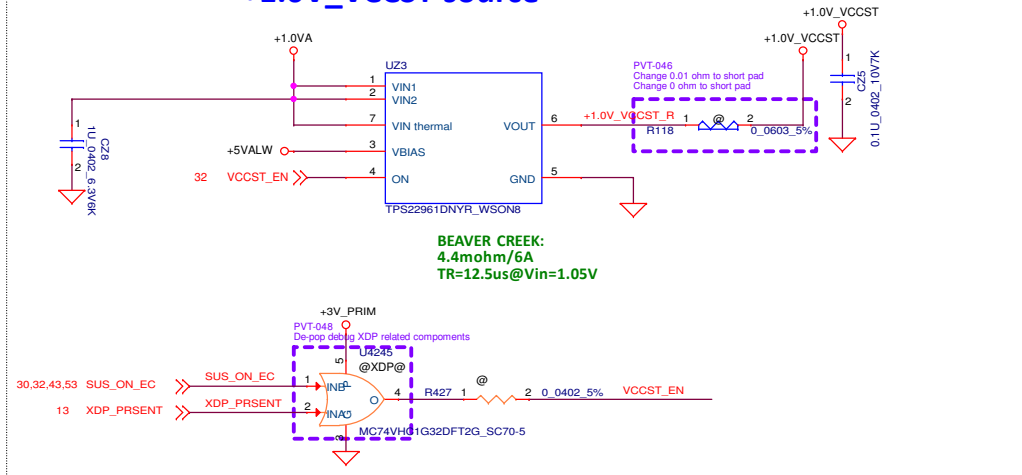
## IR CAM CONN



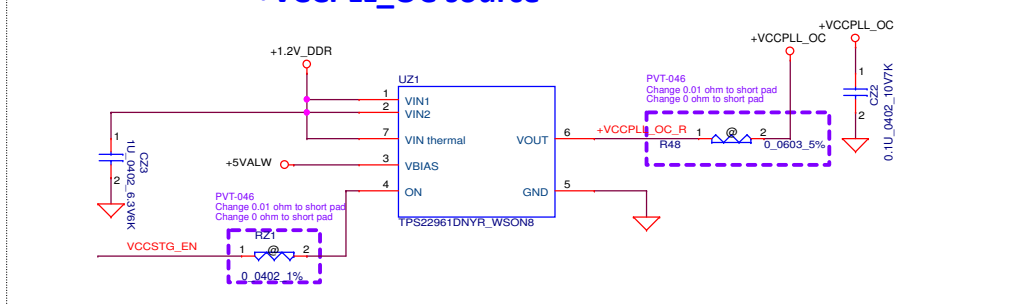




## +1.0V\_VCCST source



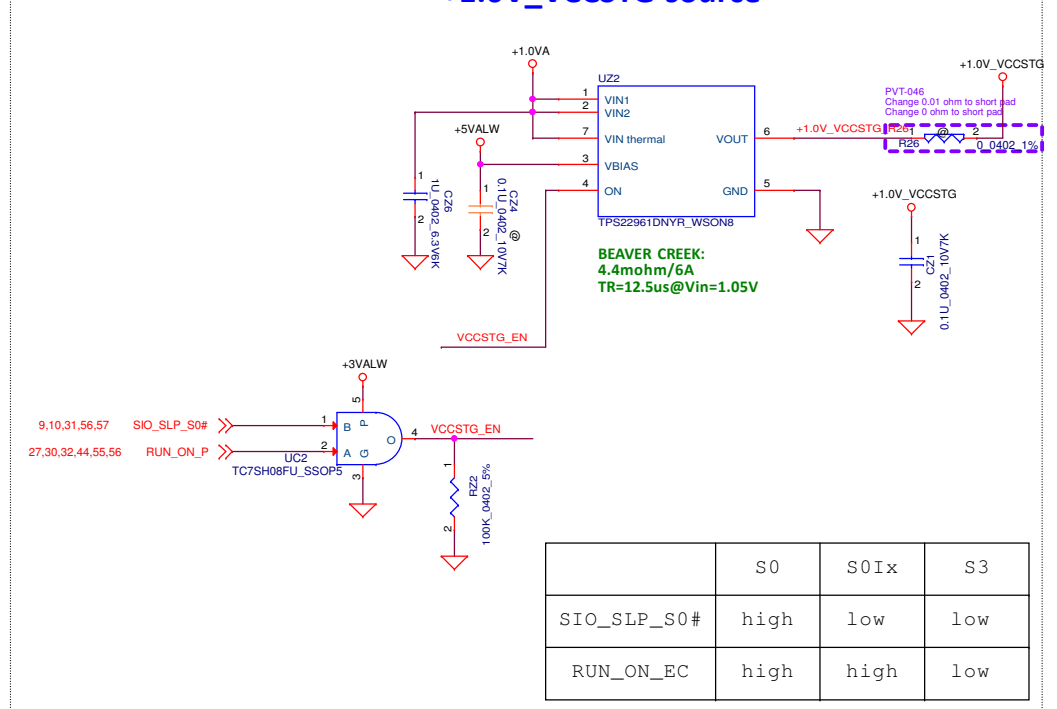
## +VCCPLL\_OC source



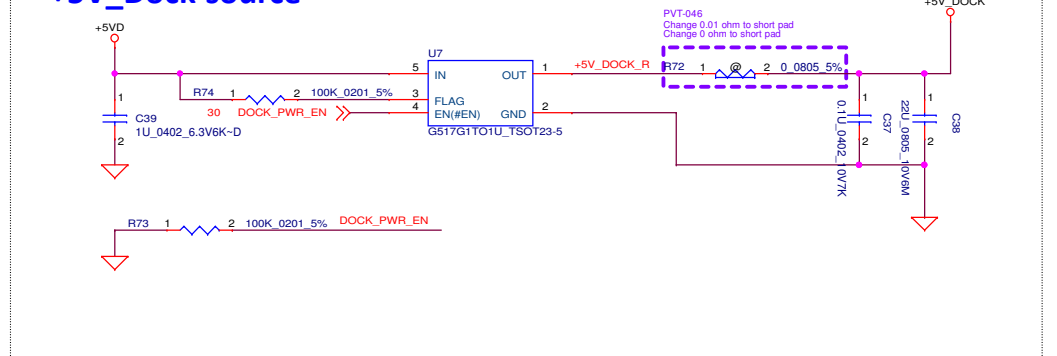
## +1.0V\_MPHYGT source



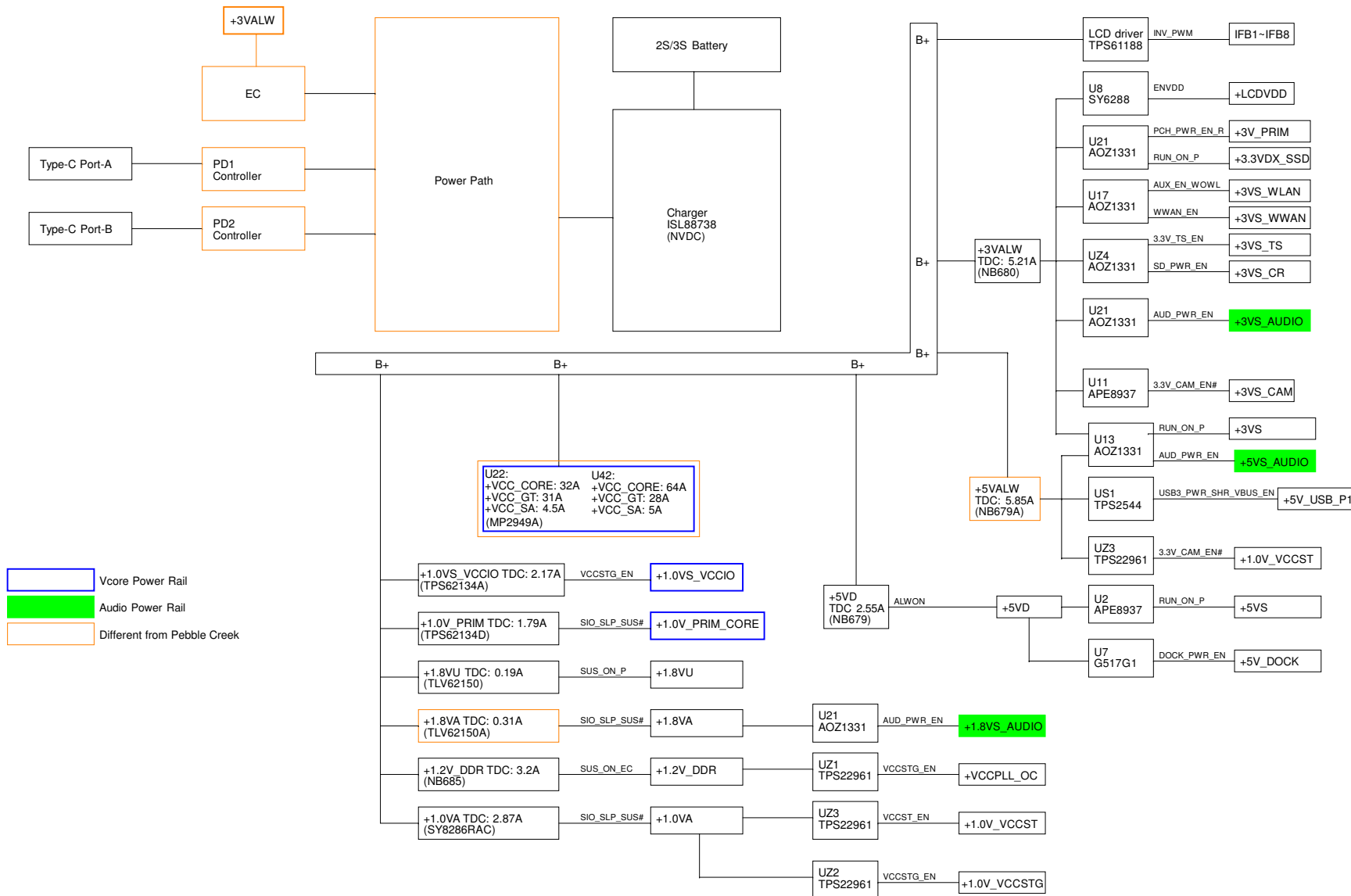
## +1.0V\_VCCSTG source



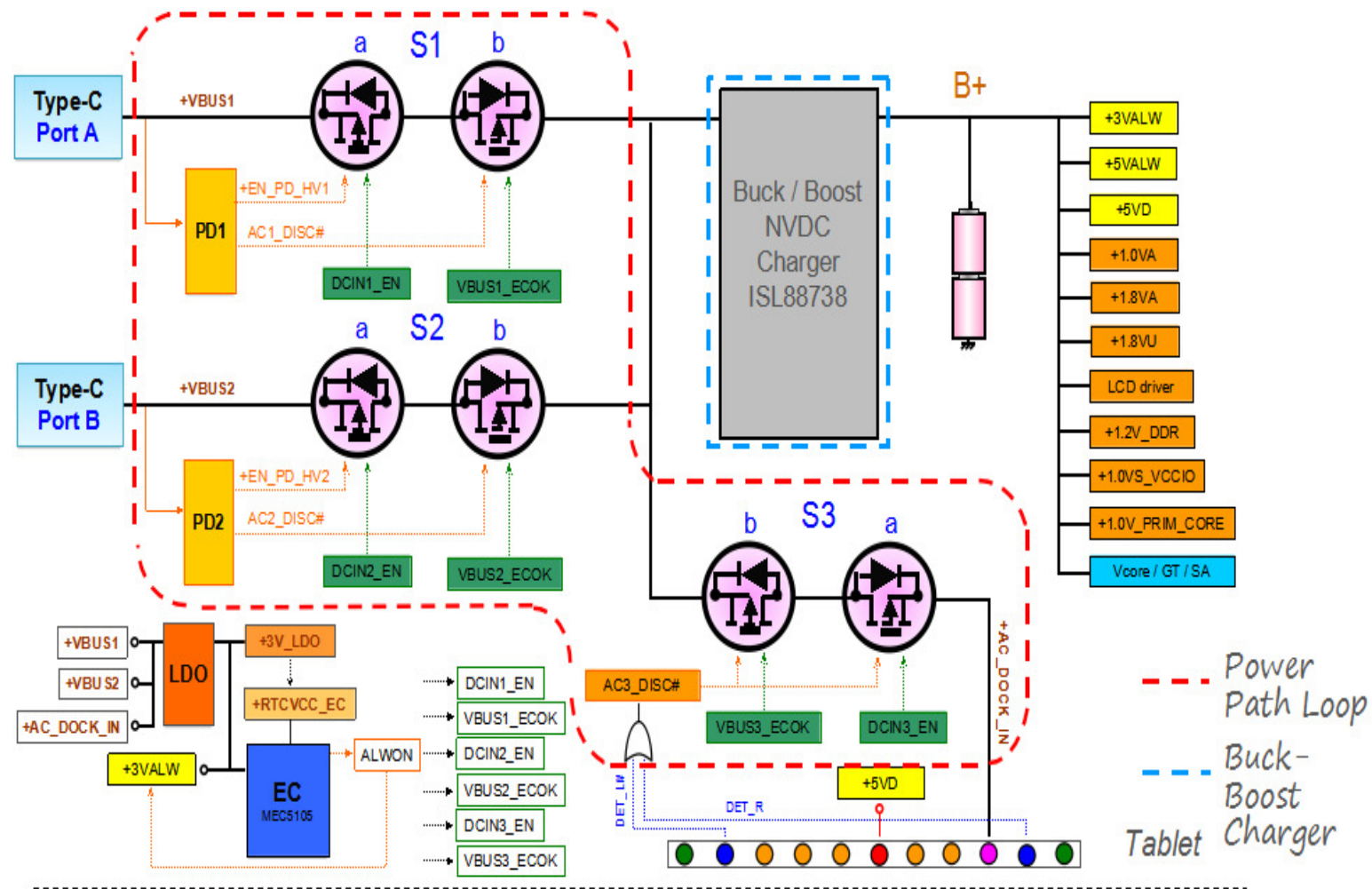
## +5V\_Dock source





# Pebble Creek MLK Power Block - Tablet



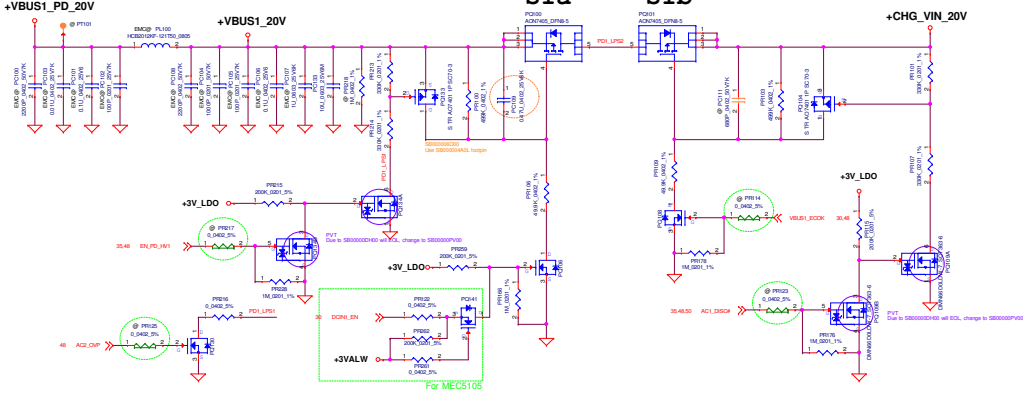
### ***Pebble Creek MLK Power Path Block***



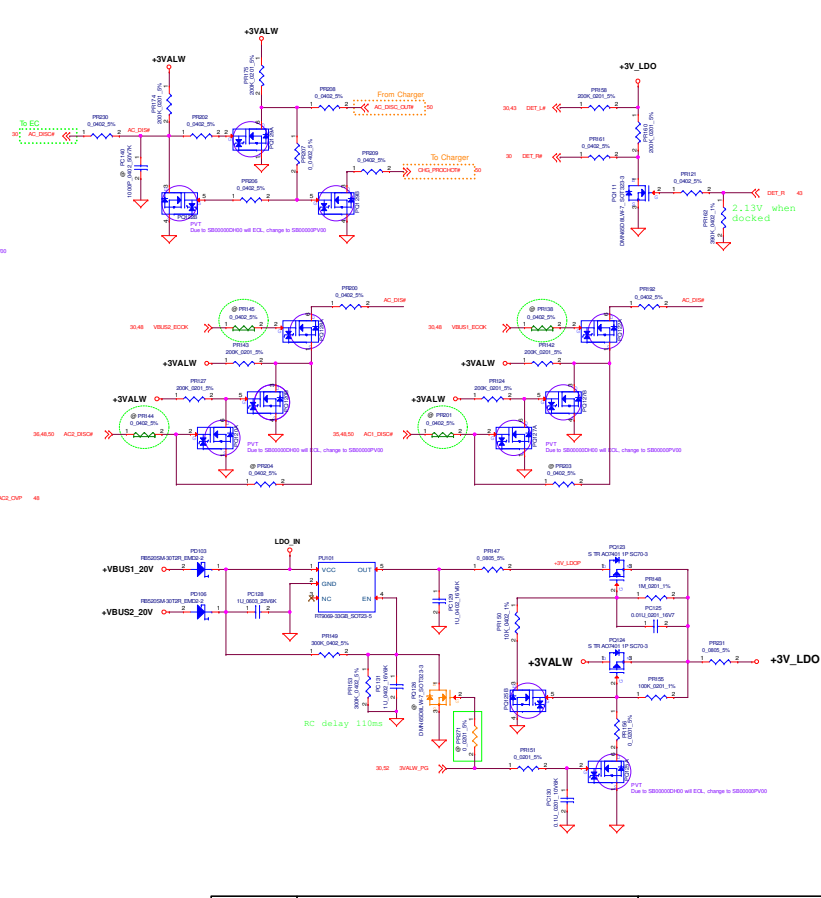
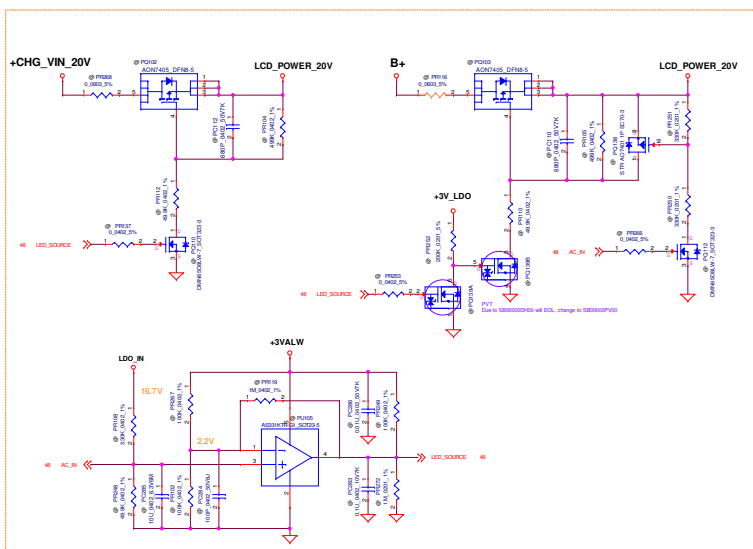
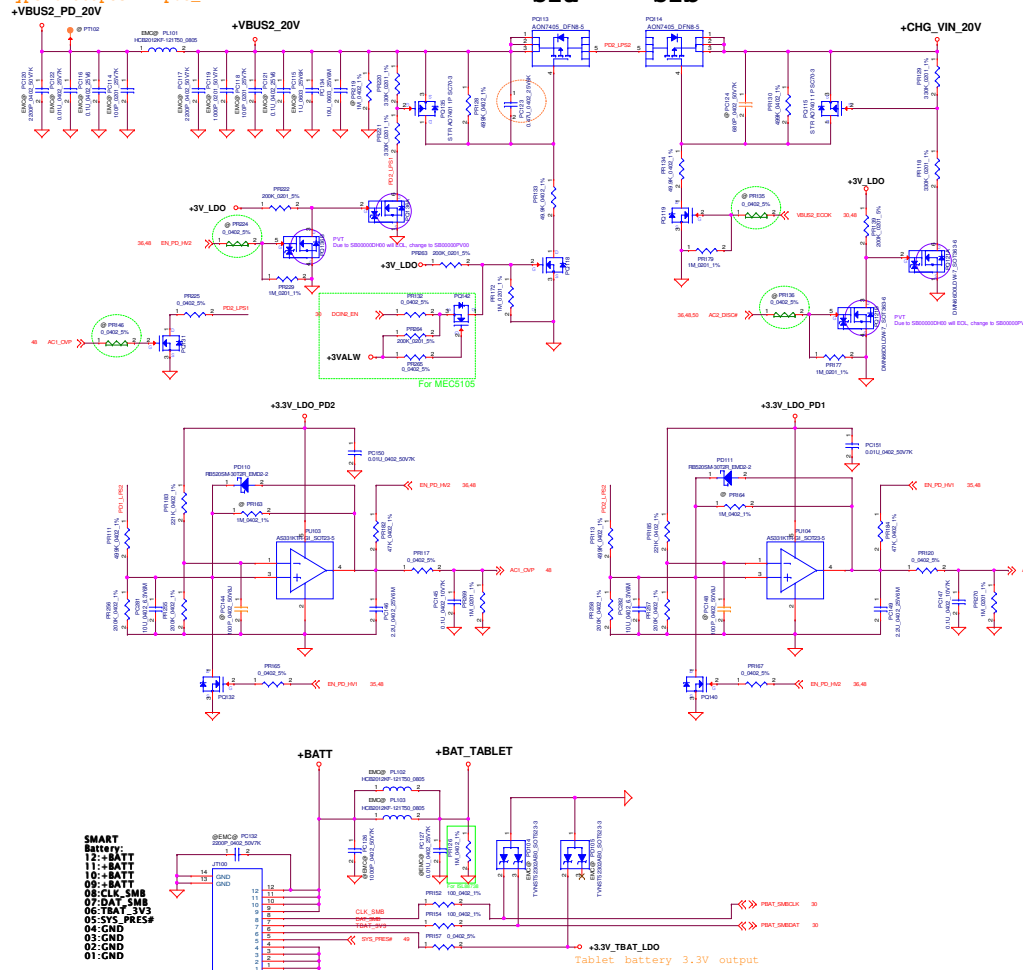
Security Classification	Compel Secret Data		<div>  <b>Compel Electronics, Inc.</b> </div>	
Issued Date	2014/06/20	Deciphered Date	2015/06/20	<div>  <b>PWR POWER PATH DIAGRAM</b> </div>
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			Date Issued, Validated by, Rev 07 01 00	

Function feild:  
Power Path(37.1), EMC Part(47.1), 3VLDO(35.27/35.28)

Type C adapter input\_1

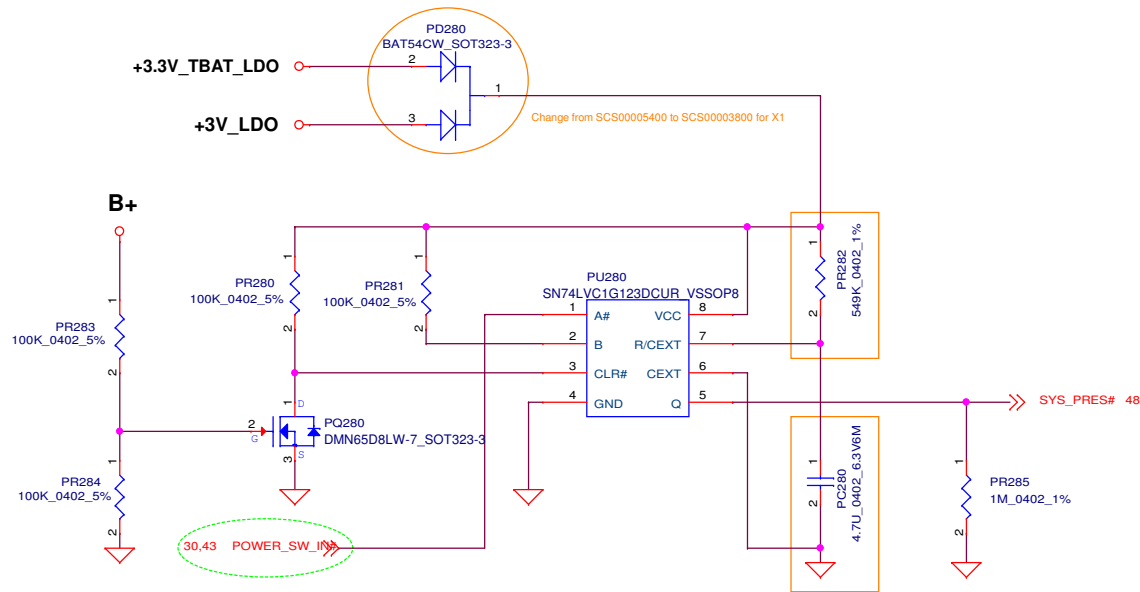


Type C adapter input\_2



SMART  
Battery:  
12: +BATT  
11: +BATT  
10: +BATT  
09: +BATT  
08: CLK\_SMB  
07: DAT\_SMB  
06: TBAT\_3V3  
05: SYS\_PRES#  
04: CND  
03: CND  
02: CND  
01: CND

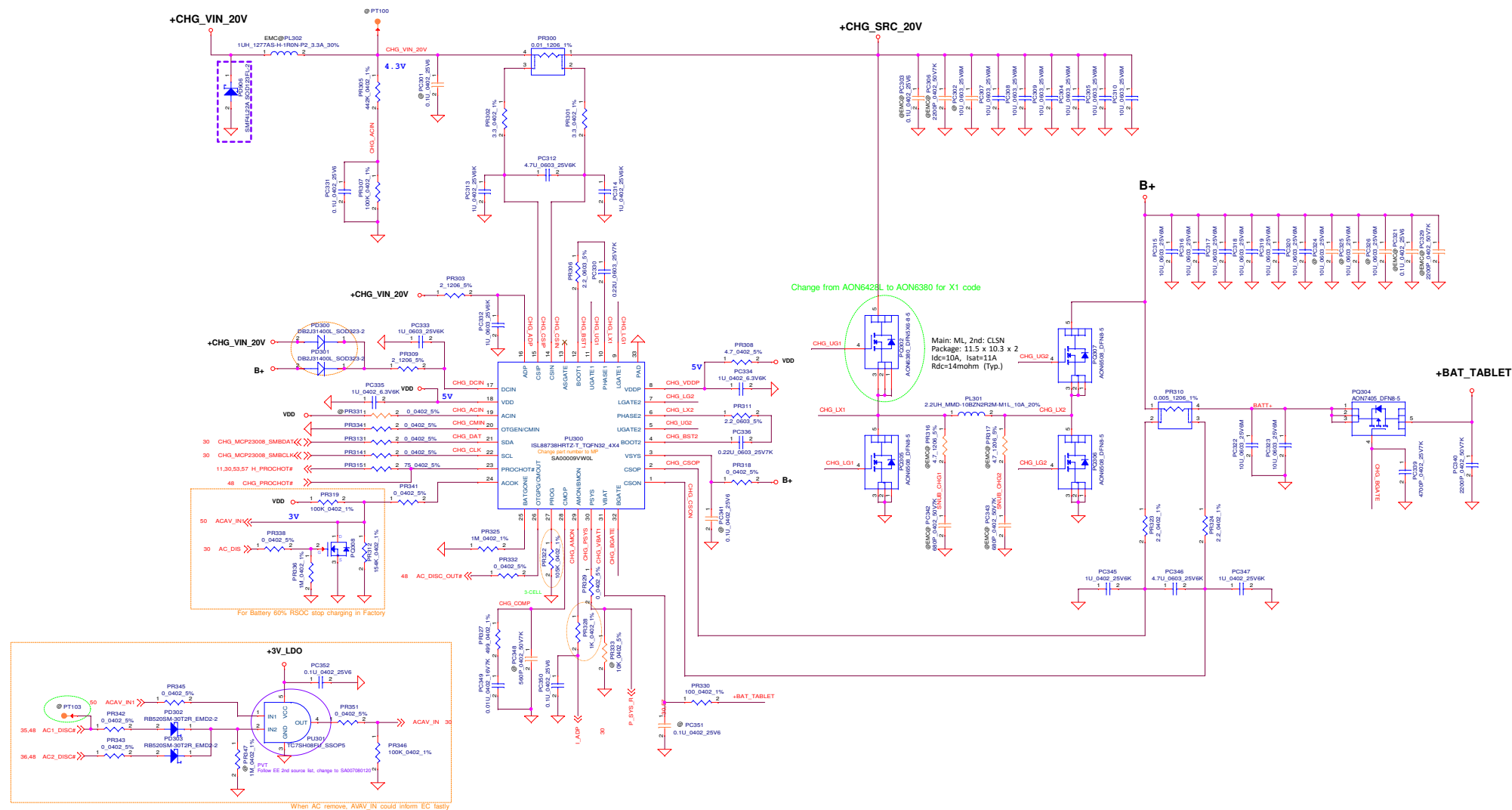
Tablet battery 3.3V output



**FUNCTION TABLE**

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L <sup>(1)</sup>
X	X	L	L <sup>(1)</sup>
H	L	↑	⌋
H	↓	H	⌋
↑	L	H	⌋

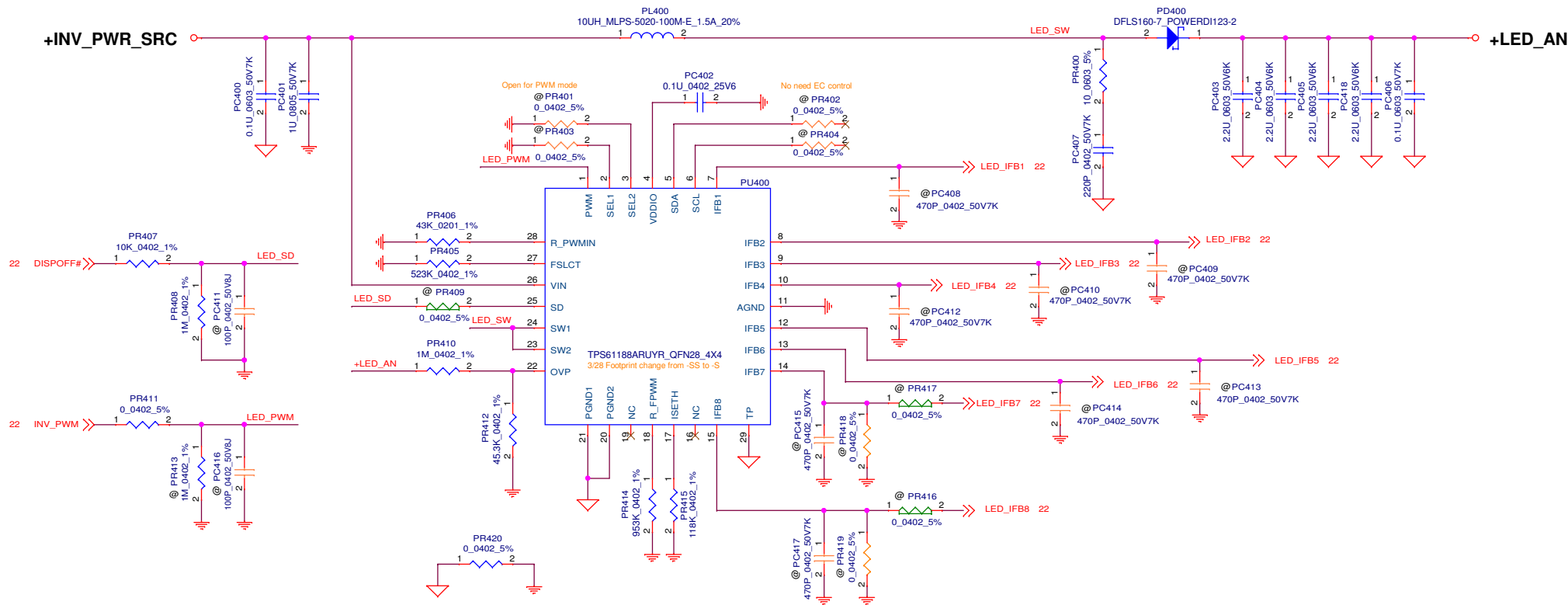
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Issued Date	2014/08/20	Deciphered Date	2015/08/20	Title	
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				Size	Document Number
				Date:	Tuesday, November 07, 2017
				Sheet	49 of 65
				Rev	1.0



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR Charger (ISL88738)</b>	
Issued Date	2014/10/24	Deciphered Date	2015/08/31	Title	
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				Date	Volume: November 09 2013 Issued: 60 of 68

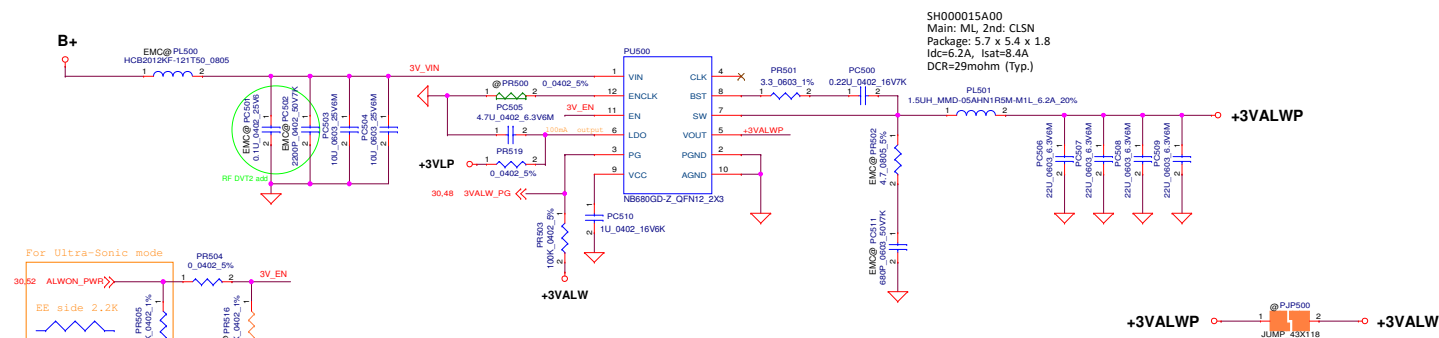
LCD driver controller(35.31), Support component(35.32)

Current:  $11.1\text{mA} \times 8 = 88.8\text{mA}$   
Max Voltage:  $6.2\text{V} \times 6 = 37.2\text{V}$

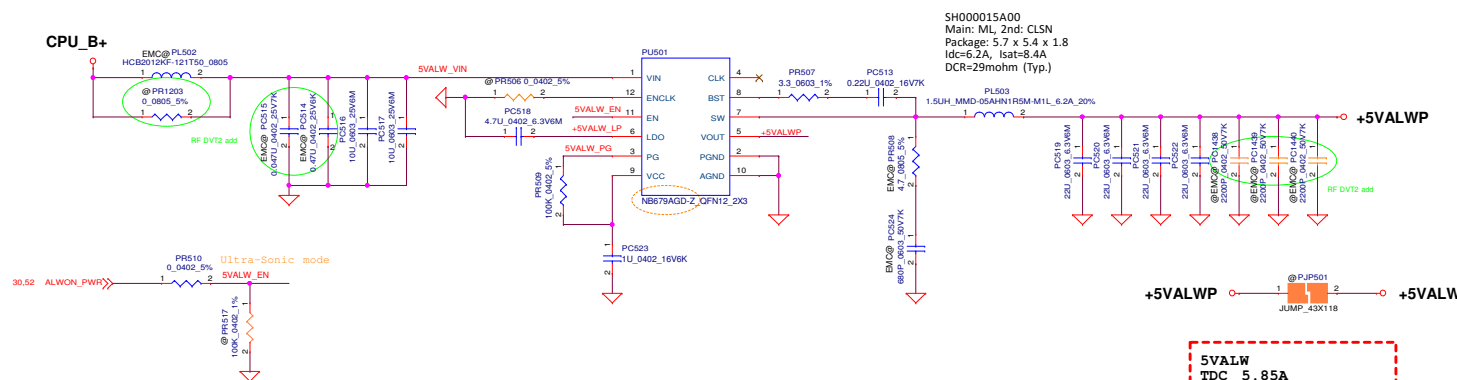


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2013/10/28		Title		PWR LCD driver (TPS61181A)	
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Date:		Tuesday, November 07, 2017		Sheet	
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3V/5V controller(35.1), Support component(35.2)



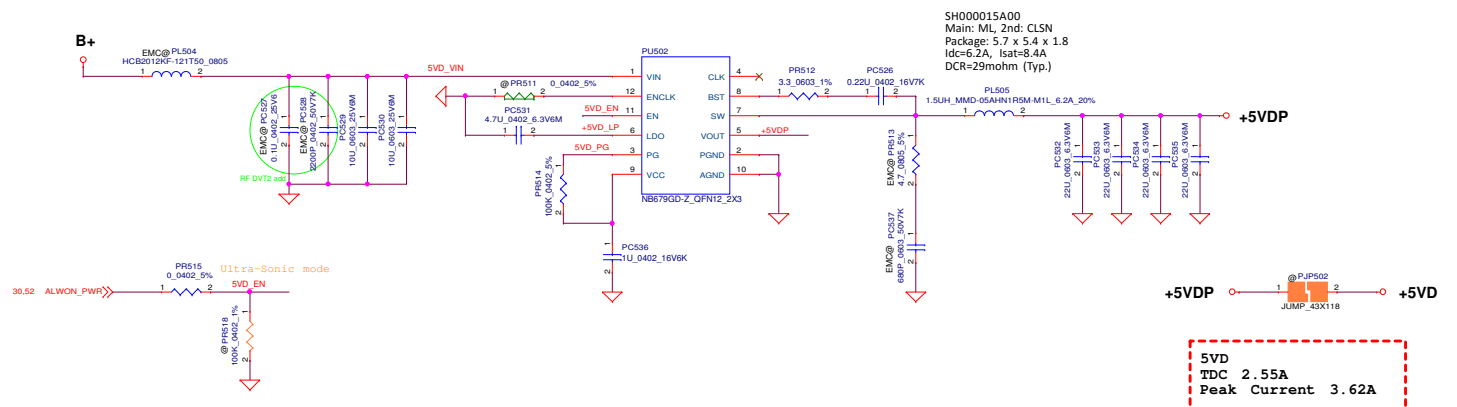
```
3VALW
TDC 5.21A
Peak Current 7.45A
```



```

TDC 5.85A
Peak Current 8.83A

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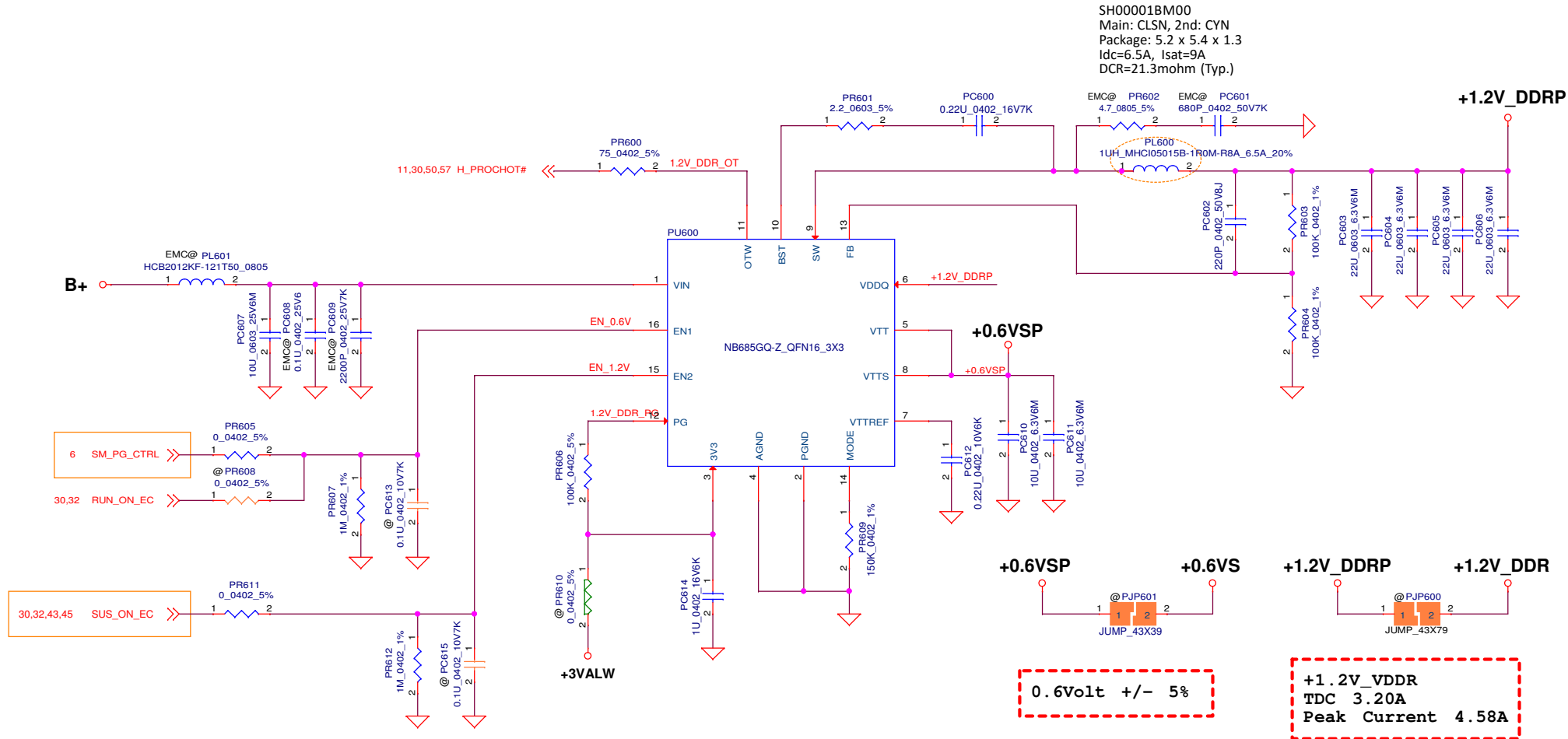


```
5VD
TDC 2.55A
Peak Current 3.62A
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Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	<b>Compal Electronics, Inc.</b> <b>PWR +3V(NB680)+5V(NB679)</b>	
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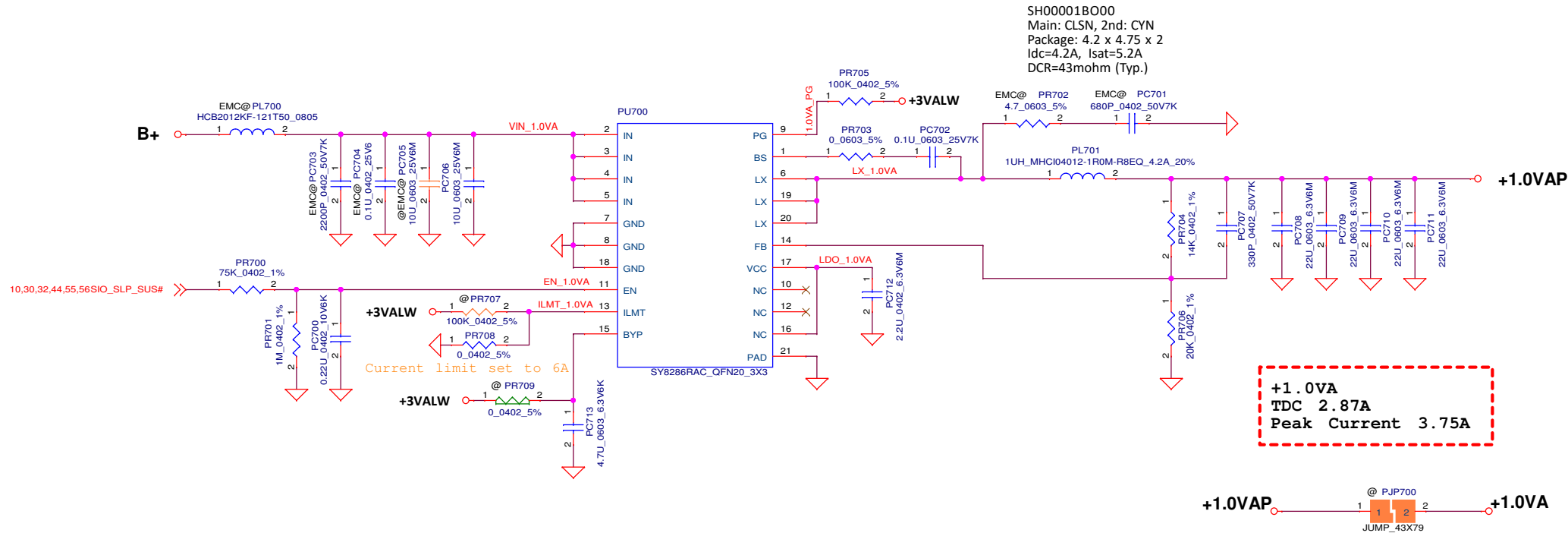
+1.2V\_DDR controller(35.3), Support component(35.4)



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				1.0	

Module Design

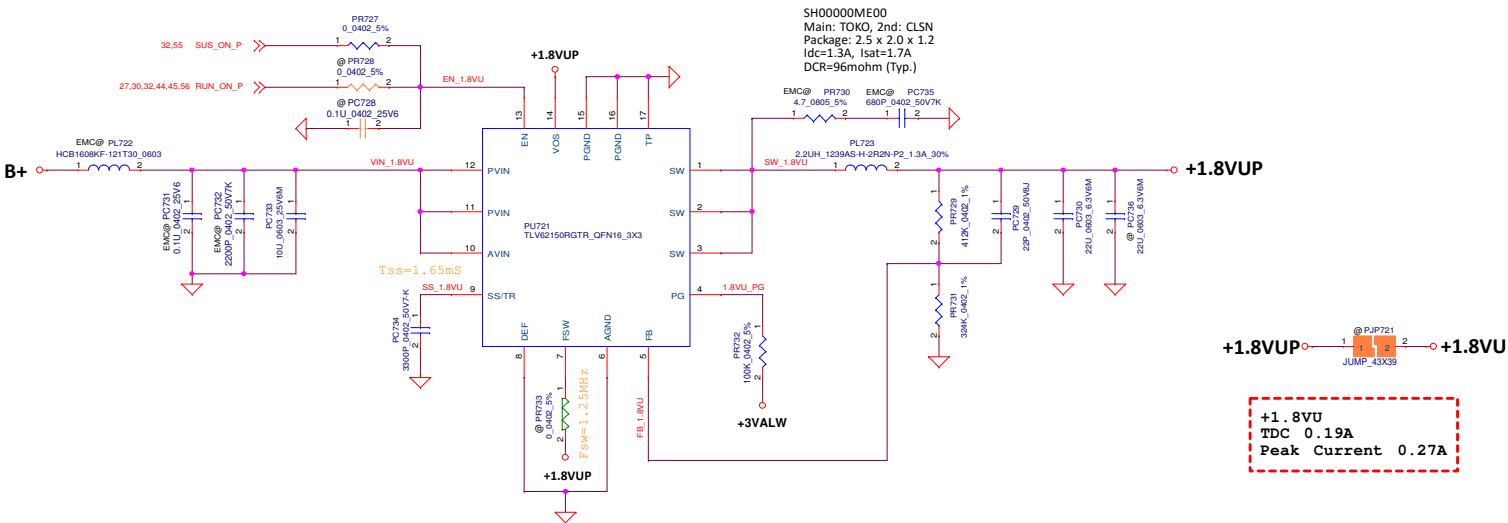
+1.0VA controller(35.5), Support component(35.6)



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		LA-F371P		1.0	

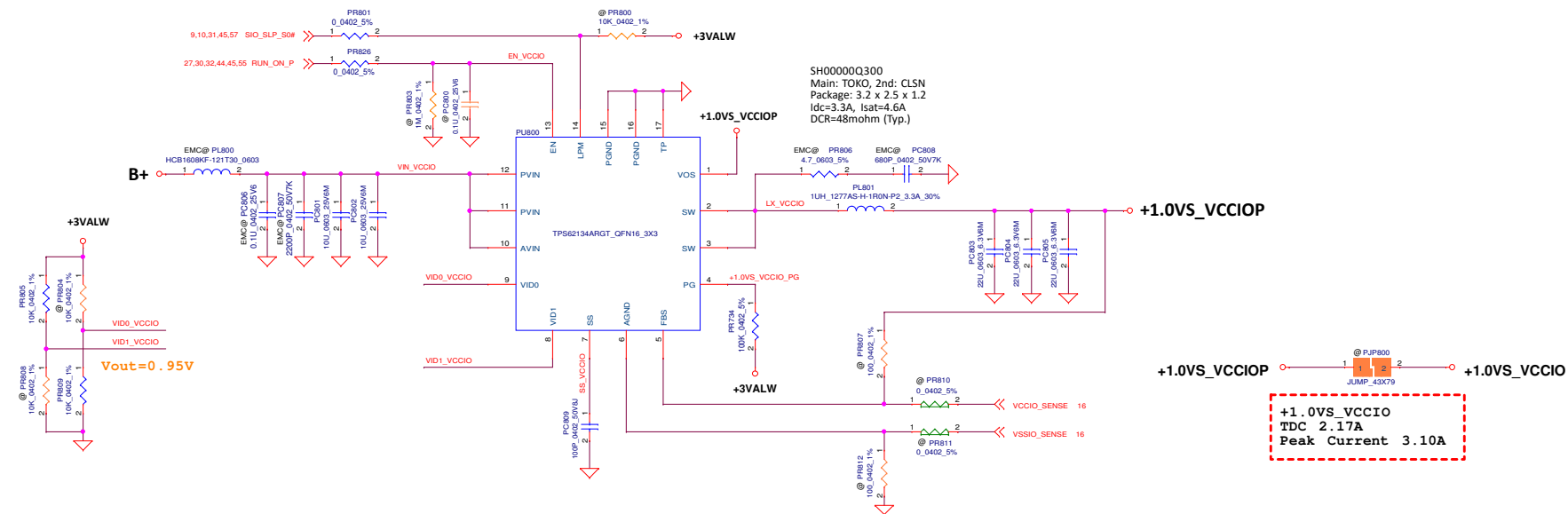
## Module Design

+1.8VU controller(35.15), Support component(35.16)

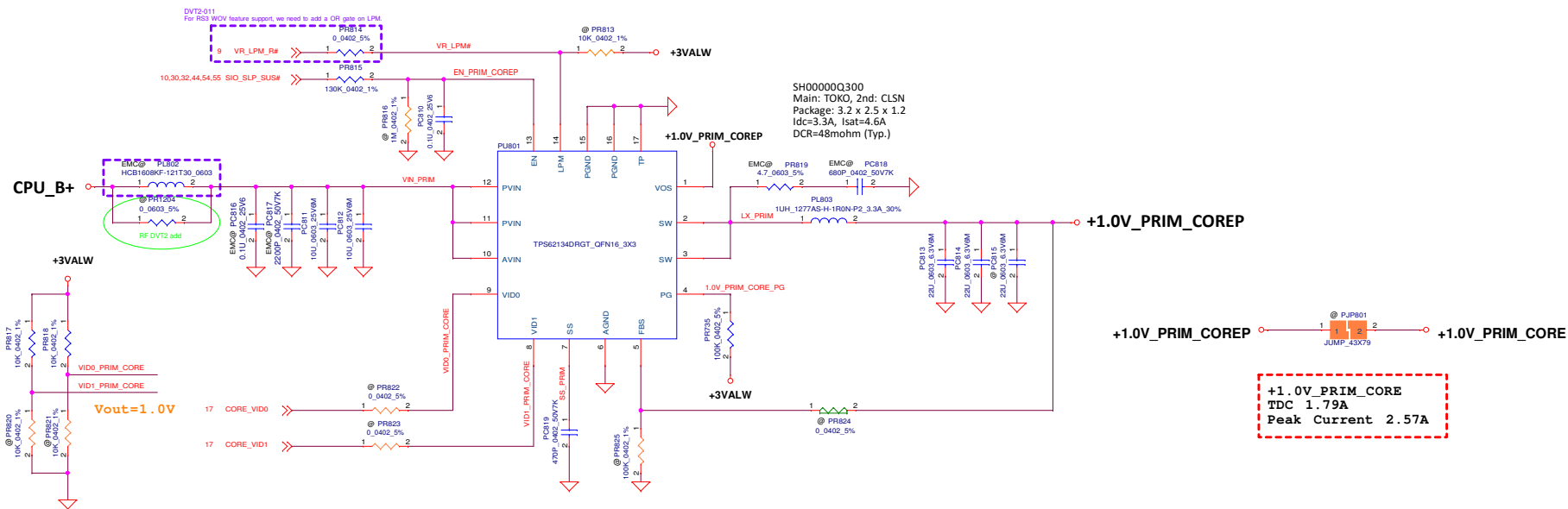


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+1.0VS\_VCCIO controller(35.11), Support component(35.12)



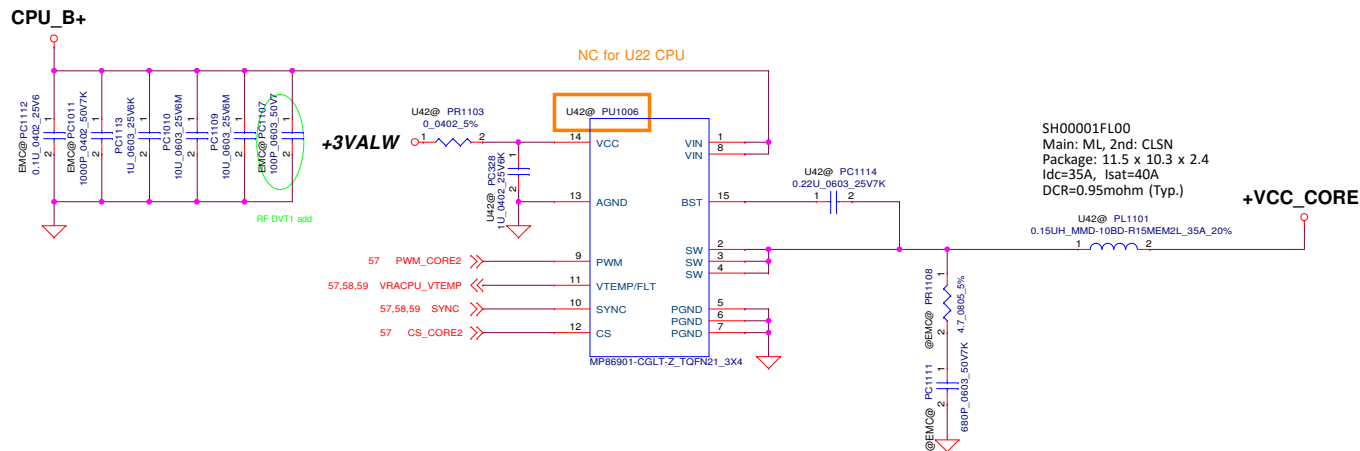
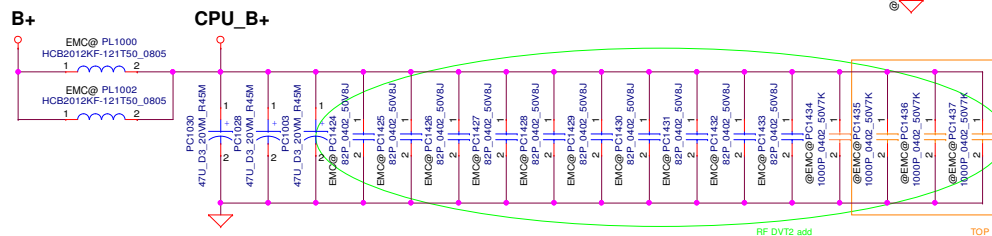
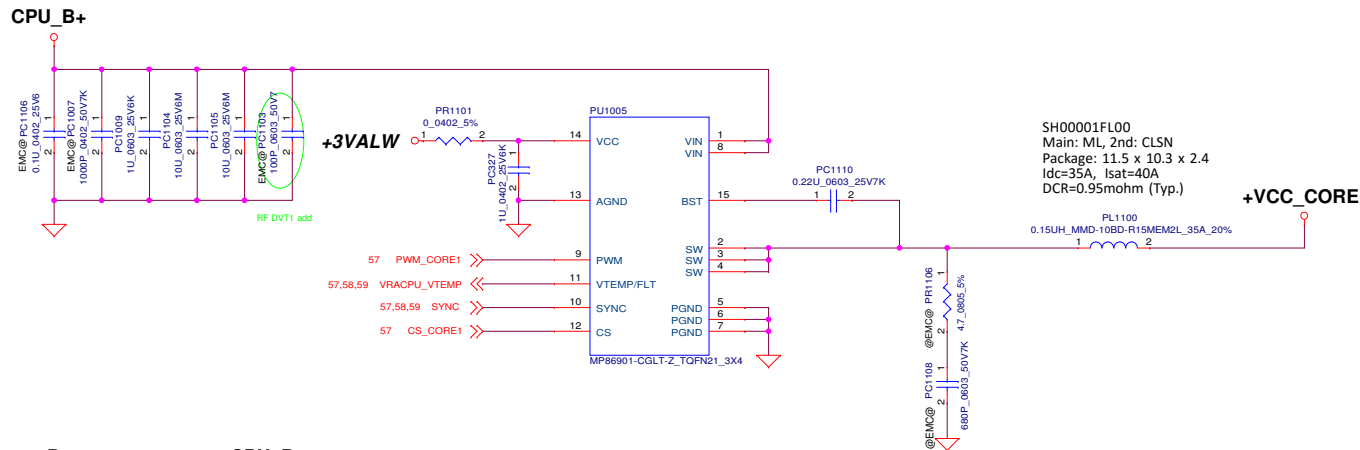
+1.0V\_PRIM\_CORE controller(35.7), Support component(35.8)



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				PWR VCCIO/PRIM(TPS62134*2)	
				Size	
Document Number		LA-F371P		Rev 1.	
Date:		Tuesday, November 07, 2017		Sheet 56 of 65	

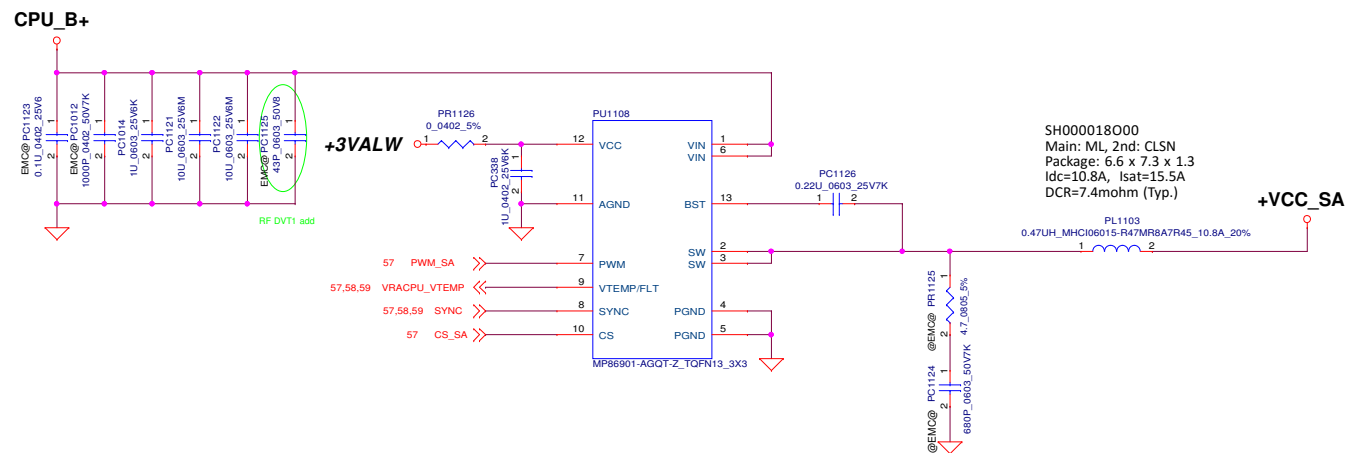
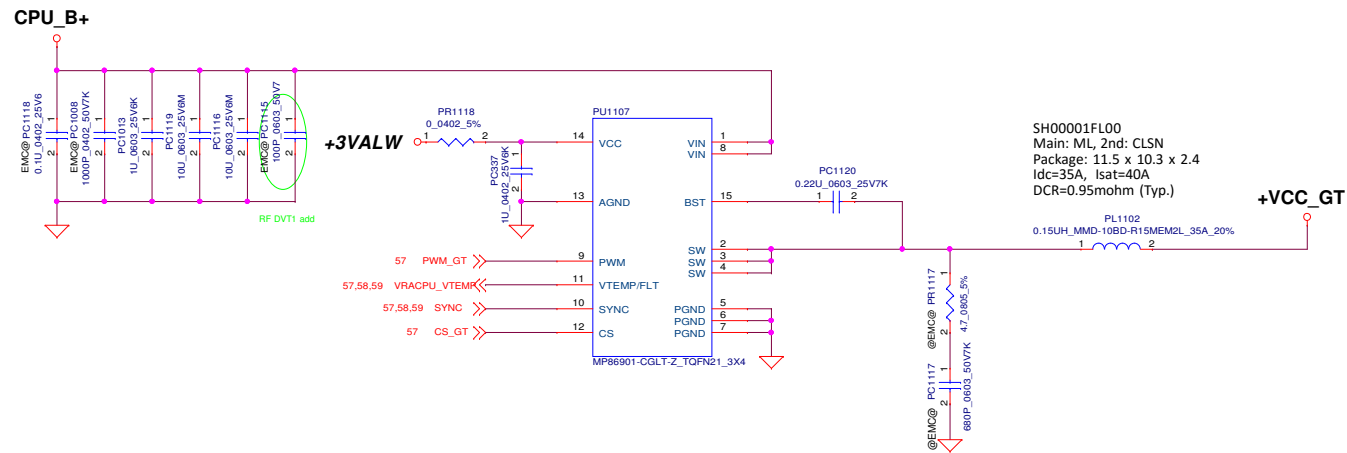


VCC\_CORE Dr. MOS (36.2), Support component(36.3)



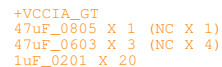
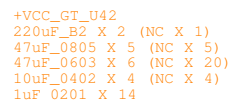
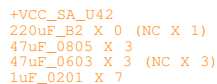
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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VCC\_GT/SA Dr. MOS (36.2), Support component(36.3)



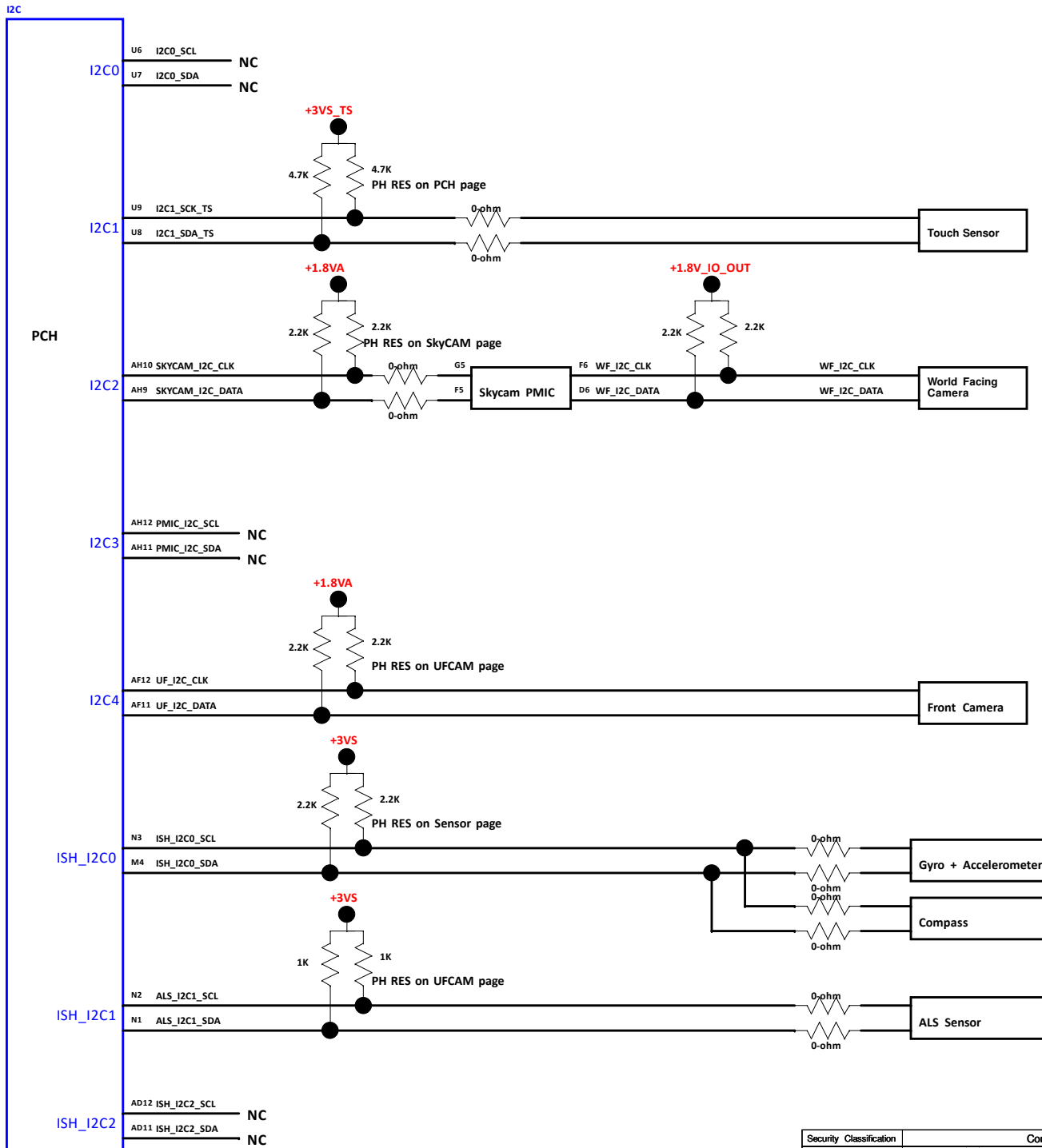
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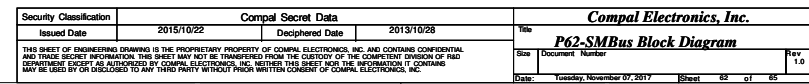
VCC\_CORE output cap(36.4), VCC\_GT output cap(36.5), VCC\_SA output cap(36.6), VCCIA\_GT out cap(36.7)



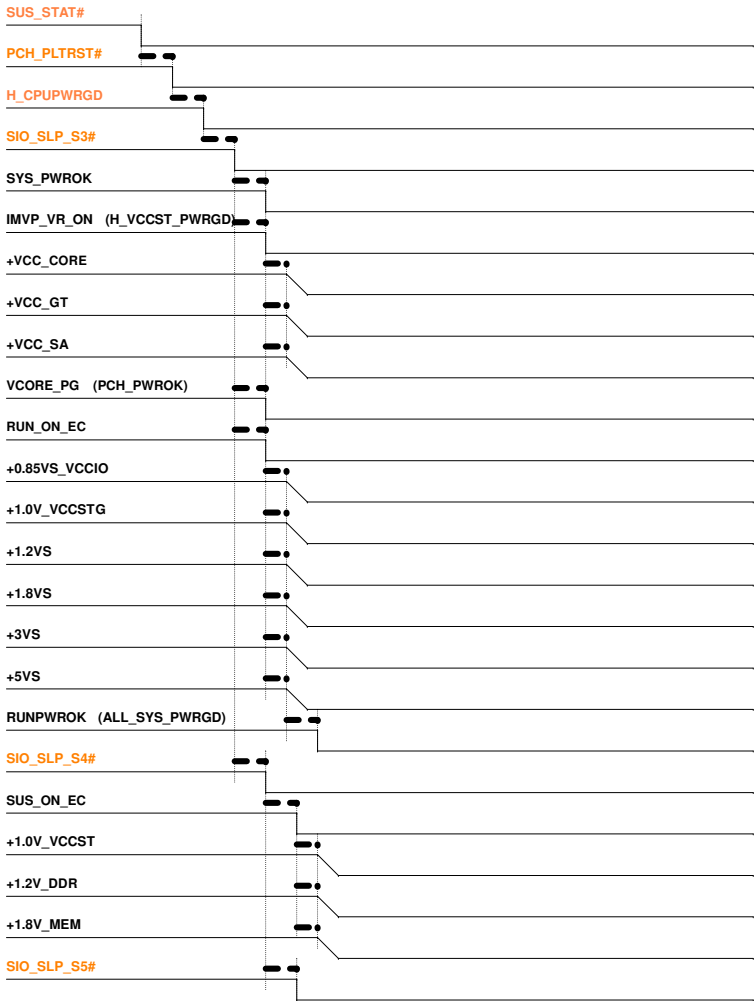
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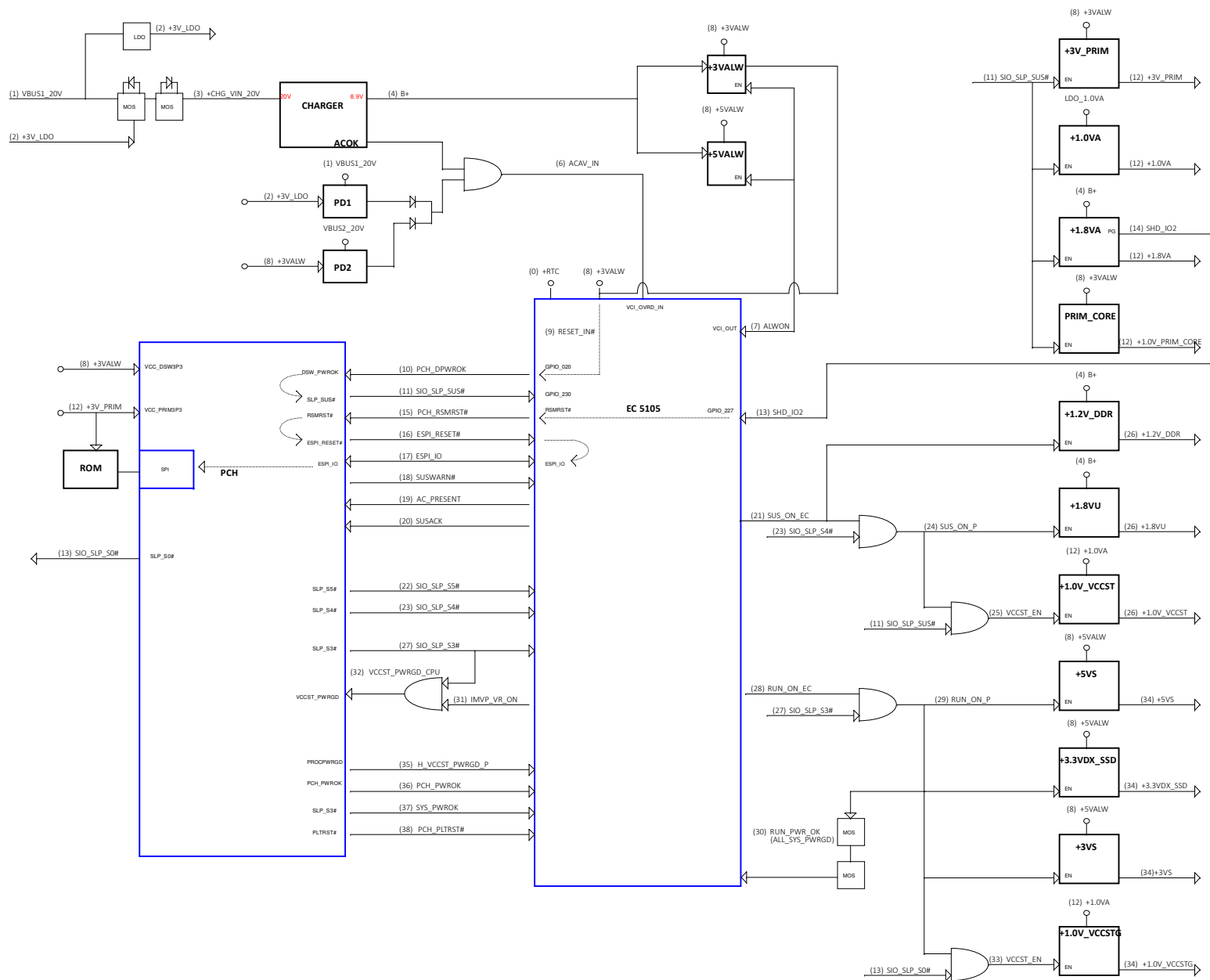












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				Rev	1.0
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				Approved	Release